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Paper Title: Partial Discharge Testing of Defects in Dielectric Insulation Under DC and Voltage Ripple Conditions

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Abstract**:** This paper details testing conducted on selected void defects in dielectric insulation samples under various HVDC voltage conditions. The aim of this work is to illustrate the type of PD activity that could be observed in HVDC insulation systems. Initially the samples were subject to HVAC excitation to confirm the defect type and establish the PD inception voltage. HVDC testing was then conducted using a 'ramp and hold' test technique with different hold voltages in the ramp determined from the measured HVAC inception voltage. The effect of harmonic ripple superimposed on the HVDC voltage waveform, which is typically a result of the converter switching operation, was also investigated. The findings from this study should provide network operators and insulation manufacturers a greater insight into the behavior of PD phenomena in solid insulation under HVDC conditions, enabling greater confidence in the diagnosis of defect type and severity in such systems.

Index Terms**:** HVDC Insulation, Partial Discharges, Power cables.

1. Introduction

HVDC transmission is increasingly being used in power systems. Conventional AC transmission in cables is limited by losses to about 50-100 km [1], beyond which HVDC transmission becomes the more cost-efficient solution. In the UK, HVDC applications include the transmission of power from isolated renewable generation sources, providing increased power flows in subsea cables from Scotland to England and enabling power trading between the UK and neighboring countries. Any system downtime will result in significant costs in terms of repairs, lost revenue and regulatory fines. The service experience for HVDC cable systems for land and subsea applications was outlined in [2]. Monitoring the condition of HVDC systems is one way to ensure that any system downtime can be planned in advance and mitigation measures put in place. The publication by Mazzanti *et al* provides background information on the behavior of HVDC insulation [3]. Recent guidelines [4] detail best working practices for the testing and diagnosis of faults in polymeric materials for HVDC insulation systems from initial design to final implementation. One method for monitoring the condition of the insulation is to detect partial discharges (PD). PD is generally produced when a defect is present or when insulation degradation occurs over time. PD detection is a well-established tool for insulation monitoring at AC voltages. In HVAC equipment, several different PD detection techniques are available depending on the application. However, PD still remains a complex phenomenon that poses challenges for measurement and diagnosis. In comparison, PD detection under HVDC conditions has received less research attention. A useful introduction to PD in HVDC insulation can be found in [5]. More recent publications on PD detection under HVDC conditions are [6]-[8].

This paper aims to further the understanding of PD measurement and analysis in solid dielectrics under DC conditions and DC with superimposed voltage source converter (VSC) ripple. PD pulses under these

conditions are characterized in terms of their magnitude and time of occurrence and a number of classification techniques explored. The main methods applied to classification at HVDC have been based on the statistical analysis of PD pulses [9-12]. Section 11 of IEC 60270 [13] details analysis methods for DC PD data. These include four methods of representing statistical PD characterization of HVDC PD data, which are utilized in Section 4 of this paper.

The PD sources used in this study were initially energized using AC to record their phase-resolved PD activity and inception voltages. DC testing was then performed considering the inception voltages under AC and using a ramped voltage technique. In separate experiments, the effects of VSC ripple on PD characteristics of a void in solid insulation were investigated. Tests were carried out using a high voltage amplifier to produce a DC voltage with superimposed harmonic ripple typical of a 6-pulse converter. The effect of the harmonics on time domain features, particularly PD pulse repetition, were explored. Quantifying the variation in pulse repetition with harmonic amplitude is proposed to generate comparative PD data for field stressing conditions of the PD test objects that are more akin to those realistically expected on an in-service cable.

Two common methods used in the analysis of PD under AC conditions are phase resolved PD (PRPD) plots and pulse sequence analysis (PSA). PRPD analysis is used in this paper to confirm the PD characteristics of the dielectric samples. Two key parameters of the PD events are required to produce a PRPD plot; the apparent charge and a phase reference angle relative to the power-frequency sinusoid. The phase location and relative spread of the PD activity are used for the identification of defect types [14]. In contrast, under DC conditions, PD generally occurs less frequently and is more likely to occur with a rate-of-change of voltage [5]. The parameters available in the analysis of PD under DC excitation are the apparent charge and the time of occurrence. The analysis of these parameters is best suited to statistical techniques. This study applies the statistical analysis techniques of IEC 60270 to demonstrate the PD behavior of defects inside a dielectric under HVDC conditions.

2. Theory

Fundamental differences exist in the mechanisms that drive PD under AC and DC applied voltages. While AC PD phenomena are well understood through lab and field experience, more research is needed into diagnostic interpretation of the phenomena under DC conditions.

2.1. AC PD

PD activity under AC conditions can be modelled by using capacitors to represent the bulk properties of the insulation system. A common model used to represent AC PD resulting from a void in a solid dielectric is the three capacitor model [5]. The gas filled void (Figure 1) is represented by C_c, the insulation in series with the void is represented by C_b and the remaining insulation is represented by C_a. Under AC conditions the voltage polarity reverses every half cycle. When the electric field in the cavity exceeds the PD inception level, a PD will occur. As the capacitance of the void discharges, the voltage across the void drops. The reliance of PD activity on the applied voltage leads to a phase-synchronization of PD activity under AC conditions.

PLACE FIGURE 1 HERE

2.2. DC PD

Under DC conditions the voltage is generally constant thus the three-capacitor model would reach steady-state and activity would cease. The DC PD model requires adaptation (Figure 2) of the AC

model to reflect the charge dissipation from the void defect into the surrounding dielectric [5]. This is achieved through the addition of resistors in parallel with each capacitor. Under DC conditions the repetition rate of PD is dependent on the applied voltage magnitude and the conductivity of the insulation surrounding the void.

In contrast to AC, PD under DC conditions has no phase reference thus characterization must be based upon correlating PD magnitude with other quantities such as time of occurrence or time-difference between consecutive pulses. At DC, discharges take place in the manner of a relaxation oscillator, where the field in the cavity is built up through charging of the capacitive defect through the leakage resistance of the dielectric, with amplitude and rate of discharge being in proportion to the magnitude of the applied voltage.

PLACE FIGURE 2 HERE

3. Methodology

3.1. AC Testing

AC tests were performed using the calibrated IEC60270 standard measurement system shown in Figure 3. The test circuit comprises a 100 kV PD-free transformer, the sample under test (represented by the capacitance C_t), a coupling capacitor (C_k) and measuring impedance (Z_m). The bandwidth of the measurement system was 100 – 400 kHz.

PLACE FIGURE 3 HERE

The AC tests were performed by incrementally increasing the voltage of the AC supply until sustained PD was apparent from the sample under test. The inception voltage was deemed to be the voltage at which repetitive and sustained PD was observed [14]. PD activity at the inception voltage was then recorded over a 10 second period in phase-resolved format by the IEC 60270 measurement system. These AC tests served to confirm the dominant source of PD for each of the dielectric samples.

3.2. DC Testing

The test circuit illustrated in Figure 4 includes the DC power supply, an input resistance R_{in}, a coupling capacitor C_k and the sample under test C_t. PD pulses were recorded using the same IEC PD measurement system used for the AC tests. The sensor connected to the measurement system was a high frequency current transformer (HFCT) with a nominal transfer impedance of 4.3 Ω and a bandwidth of 100 kHz – 20 MHz. A pulse injection calibration unit was used to ensure the output from the HFCT could be quantified as an apparent charge on the IEC 60270 measurement system.

PLACE FIGURE 4 HERE

A key feature of the DC test procedure was the ramp test profile [15]-[16]. The ramp test uses the peak value V_R of the AC inception voltage as a basis for defining the voltage variation with respect to time. The ramp tests consisted of three voltage increments (as shown in Figure 5) after which the voltage was held constant at $V_R/2$, V_R and $3V_R/2$ for 30 minutes each, followed by a final ramp down period of 30 seconds from $3V_R/2$ to 0 V. The data under analysis in this case is the 30-minute hold data recorded after each of the 3 voltage steps.

PLACE FIGURE 5 HERE

Section 11 in IEC 60270 recommends two methods for evaluating DC PD test data. Firstly, recording

the pattern of consecutive charge pulses for a PD test period of 30 minutes at constant DC test level. Secondly, determining the cumulative PD pulse charge recorded over the 30 minutes PD test period. Two further methods are recommended for performing statistical analysis on the PD data. Firstly, measuring the number of pulses whose apparent charge exceeds a specified threshold level for the PD data under test – this was termed 'exceeding frequencies of PD pulses'. The second analysis method assesses the total number of PD pulses whose charge lies within a defined set of ranges of PD magnitude for the PD data under test – this was termed 'class frequencies of PD pulses'. These methods were applied to the PD data gathered during the 30-minute hold at $3V_R/2$.

3.3. VSC Ripple Test Method

HV waveforms were applied to insulation test samples using an arbitrary waveform generator feeding an HV amplifier, as shown in Figure 6. The maximum slew rate of the system was 750 V/µs. For the tests reported here, a DC voltage was generated with superimposed harmonics of 50 Hz power frequency having orders and relative magnitudes as listed in Table I, based on available data for a 6-pulse VSC converter [17].

PLACE FIGURE 6 HERE

PLACE TABLE I HERE

To test its effect on time-domain PD features, the 6^{th} harmonic voltage content was varied with respect to the HVDC voltage, while higher-order harmonics (12^{th}, 18^{th}, 24^{th}) were maintained at the same percentage levels relative to the dominant 6^{th} harmonic.

PD was measured with the same HFCT as that used in testing under pure DC conditions. The HFCT was clamped round the earth terminal of the insulation test sample. To correlate voltage levels and phase with PD pulse features, a voltage output monitor, integrated with the amplifier, allowed a low voltage version of the amplifier's output to be measured by the oscilloscope at a divider ratio of 3000:1.

3.4. Test Samples

Dielectric insulation samples were selected to reproduce PD that may occur in an HVDC insulation system. The samples were an epoxy resin disc with two brass plane electrodes fixed to its upper and lower faces. The first sample contained five voids (Figure 7(a)) and the second contained a single void (Figure 7(b)).

PLACE FIGURE 7 HERE

4. Results

4.1. AC Test Results

Sample (a) had an inception voltage of 8 kV rms. The IEC PD level at this voltage was 680 pC. This was a relatively high PD level, but not unexpected given the number of parallel voids in the sample and the close coupling to both external electrodes. The PRPD plot for the sample at 8 kV is shown in Figure 8. Discharges generally occur in advance of the test voltage peaks, a characteristic typical of internal PD [14].

PLACE FIGURE 8 HERE

4.2. DC Test Results

Results from testing the same samples under DC conditions are presented using the methods

suggested in IEC 60270 for analyzing PD under DC conditions. The PD data under analysis was gathered at the highest test voltage ($3V_R/2$), during which PD pulses were measured over 30 minutes to gather sufficient data for subsequent statistical analysis. In some cases, the maximum hold DC voltage had to be modified based on the level of observed PD activity.

The AC inception voltage for the five-void sample was 8 kV rms, giving a peak voltage of V_R=11.3 kV that was used to derive three hold voltages (5.6 kV, 11.3 kV and 17 kV) for ramp testing on sample (a). The voltage was ramped up to $3V_R/2$ (17 kV) but following the 2-minute wait period (which was necessary to ensure any that PD activity detected is not caused by the recent voltage change), only limited PD activity was detected. The voltage was increased further to $9V_R/5$ (20 kV) where 33 PD events were recorded. The plot in Figure 9(a) shows the pulses detected from the sample whilst the voltage was held at 20 kV for 30 minutes. The plot in Figure 9(b) shows the accumulated PD charge over the measuring period. Figure 10(a) illustrates the exceeding frequencies of PD pulses. Figure 10(b) shows the class frequencies of PD pulses, as outlined in section 2.2.

PLACE FIGURE 9 HERE

PLACE FIGURE 10 HERE

4.3. VSC Ripple Test Results

Sample (b) containing a single 0.6 mm diameter spherical void was used in the following tests. The sample had an inception voltage of around 4 kV DC. Tests were carried out at this applied voltage level, with subsequent measurements taken at a baseline 4 kV HVDC level with harmonic content added. These were generated with a dominant 6^{th} harmonic at 5% of the baseline HVDC voltage, then at 10%, then 15%. In all three cases, the 12^{th}, 18^{th} and 24^{th} harmonics maintained the same amplitudes relative to the 6^{th} harmonic as given in Table I. It should be noted that in Table I, it is shown that in an idealised 6-pulse converter, the dominant harmonic would have an amplitude of approximately 4 percent of the baseline HVDC voltage. In this study, we are attempting to investigate and quantify the effects on PD of these harmonics in a controlled laboratory enviromment rather than recreating a single, down-scaled, typical HVDC waveform. For the purpose of the study, we have therefore increased the relative harmonic amplitudes, varying them up to a maximum of 15 percent of the baseline HVDC level.

Figure 11 shows typical PD pulse sequences for the activated void sample at HVDC with increasing levels of harmonics (note the shorter time scale in the case of HVDC only). A well-defined time spacing between PD events was observed at pure HVDC applied voltage, typically in the region of 0.7 ms. With the addition of harmonic ripple, PD activity tends to cluster around the dominant harmonic peaks. Pulses generally increase in repetition rate and amplitude as the harmonic amplitude (and thus peak voltage) increases. In cases where harmonics were applied, it was observed that PD activity tends to oscillate between low amplitude, sub-millisecond pulse spacing and a pulse spacing of approximately 3.3 ms, as dictated by the period of the 6^{th} harmonic.

PLACE FIGURE 11 HERE

To more effectively visualize the influence of harmonics on PD pulse spacing, over 1000 data records were recorded at sampling rate of at least 250 MSs^{-1} to ensure features of the PD waveforms were accurately resolved. The time delay between each trigger event and the subsequent PD pulse (defined as ΔT) were recorded for each trace and plotted as histograms corresponding to each of the four harmonic amplitude test cases, as shown in Figure 12.

PLACE FIGURE 12 HERE

Results indicate that for the void defect tested, the voltage harmonics significantly influence the PD repetition rate, with pulse spacing matching the period of the 300 Hz 6th harmonic. This is evident by the difference in pulse spacing (ΔT) between Fig. 12(a) and 12(b). With no harmonic applied (pure DC), a narrow distribution of predictable ΔT values occurs – in this case around 0.6 ms between pulses. This would be expected from PD theory at HVDC discussed in Section 2.2, with ΔT being dictated by the properties of the insulator, applied voltage and geometry of the defect. As harmonics are added and their amplitudes increased, the pulse distribution becomes increasingly leptokurtic in proportion to harmonic voltage level, with their mean occurring around the period of the dominant harmonic. For a 300 Hz harmonic the period is T = 3.3 ms, matching the dominant ΔT observed in Figure 12(a). Since discharge rates in HVDC applications are correlated with the applied voltage (as well as the conductivity of the insulation) [18]-[19], it is hypothesised that clustering of pulses around the harmonic peaks is partly a result of the corresponding overvoltage above inception at each of these peaks. This differs from pure AC phenomena, where the dominant frequency would be twice per cycle.

5. Discussion

In the case of pure HVDC, PD was generally only measureable when the DC voltage was increased to 3/2 times the peak AC inception voltage (V_R). This is as expected from available literature [5]. Generally, no sustained PD activity was detected until the voltage was held at $9V_R/5$.

PD under AC excitation was mostly higher in magnitude and more frequent than PD from the same sample under DC conditions. The largest PD event under AC conditions was 1940 pC and the largest under DC conditions was 220 pC. In a 10 second hold under AC conditions 1970 events were recorded compared to 33 events under DC conditions over a 30 minute period. Previous studies have reported similar findings when comparing AC and DC PD activity [5]. At equivalent DC voltages, PD behavior exhibits lower magnitude and repetition rates. However, note that in this case the DC data was acquired at a higher voltage, which could contribute to the higher PD magnitude.

The methods recommended in IEC 60270 enable the PD activity to be represented in a generic way for comparison. The expansion of knowledge around DC PD testing coupled with the recommended methods would be valuable for operators of HVDC systems. The behavior of the insulation system could be characterized without implementing system shutdowns for AC testing or in systems where the HVDC system design does not allow AC energisation.

Investigation of the effect of VSC harmonic voltage ripple demonstrated that the distribution of time-intervals ΔT between pulses exhibits a strong correlation with the period of the dominant voltage harmonics that could be present as a result of the VSC switching regime. The phase relationship of PD to the harmonic voltage in HVDC applications occurs by means of a different physical process than the phase relationship of PD to the power-frequency waveform in HVAC applications. It therefore appears unlikely that existing knowledge of AC PRPD characteristics can be transferred directly for application to HVDC. It is proposed that metrics such as repetition rate and harmonic-phase correlation be investigated more extensively in future through programs of testing on defect samples under different conditions, as well as through the acquisition of on-site data.

6. Conclusions

This paper has presented AC, DC and DC-superimposed-harmonic testing of void-type dielectric samples. AC testing was used to confirm the inception voltage of PD and the dominant PD source through reference to the PRPD behavior. The AC inception voltage was used to define voltages for use in DC ramp testing of the samples.

The proposed test methods for DC PD testing were employed to statistically analyze PD data under DC conditions. These methods may augment present AC PD test methodologies and standardize test methods as DC PD diagnostics becomes more prevalent. Mapping the distribution in time differences between PD events for various levels of VSC harmonic ripple demonstrated a strong correlation with the period and amplitude of the dominant harmonic, with the higher amplitude PD events tending to occur around the harmonic peaks with increasing probability as the depth of harmonic modulation voltage was increased. Harmonic distortion has become progressively more noteworthy as the ratings of HVDC installations have increased. While this, in itself, is an undesirable phenomenon, results indicate that it may be useful from a diagnostic standpoint since it provides a reference for potentially correlating PD features that may yield identifying characteristics for defect type and severity.

7. Acknowledgement

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Minan Zhu Minan is a research assistant at the high voltage technologies laboratory in the University of Strathclyde. He has worked on a number of projects related to partial discharge testing in medium voltage cables, transformer PD location analysis and UHF PD signal conversion to IEC standard apparent charge. Minan also conducted research on energy harvesting in electric fields.

Martin Judd graduated from the University of Hull in 1985 with a BSc (Hons) in Electronic Engineering, followed by 8 years of industrial experience with Marconi Electronic Devices and then EEV. He received a PhD from the University of Strathclyde in 1996 for research into the excitation of UHF signals by partial discharges in gas insulated switchgear. Martin has worked extensively on partial discharge location techniques for power

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Malcolm Seltzer-Grant received a BEng (Hons) degree in Electrical and Electronic Engineering from The University of Manchester in 2005. Since 2005 he has been with HVPD whilst studying for a PhD degree at The University of Manchester School of Electrical and Electronic Engineering which was awarded in 2010 for research into measurement techniques and applications of on-line partial discharge detection in power cables. At HVPD he works in the development of PD test and monitoring devices.

Riccardo Giussani was born in Legnano, Italy. He graduated as an electrical engineer from Politecnico di Milano, Italy and completed a PhD at The University of Manchester, UK. Since 2013 he has been working as Senior Development Engineer at HVPD Ltd, UK.

Figures:

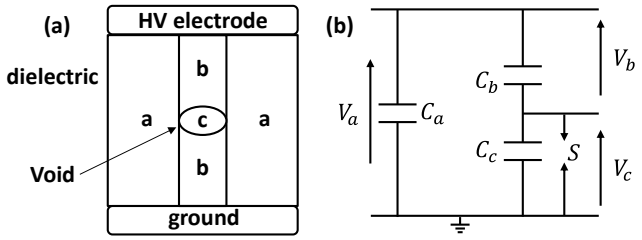

Figure 1. (a) Illustration of void type defect indicating which sections of insulation correspond to which capacitances and spark gap (*s*). (b) Three capacitor model for AC PD.

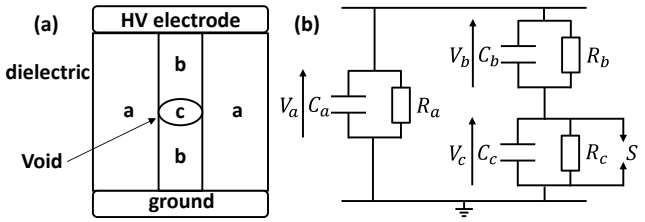

Figure 2. (a) Illustration of void type defect indicating which sections of insulation correspond to which capacitances, resistances and spark gap (*S*) (b) Three capacitor model adapted for DC PD.

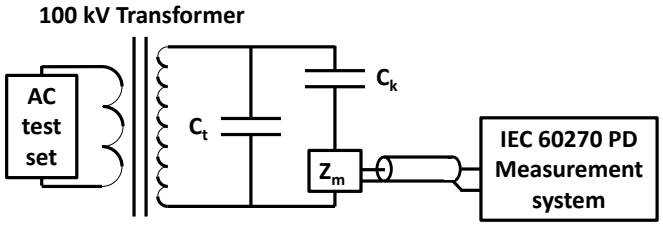

Figure 3. AC test circuit with IEC 60270 detection system. The circuit consists of a C_t the sample under test, C_k the coupling capacitor and Z_m the measuring impedance connected to the IEC 60270 PD measurement system.

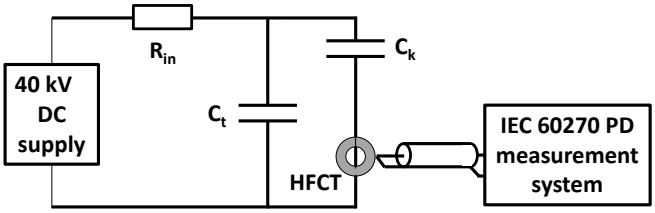

Figure 4. DC test circuit with HFCT and IEC 60270 PD measurement system. Resistance R_{in}=25 MΩ, C_t is the sample under test, C_k is the coupling capacitor of 1.9 nF and the HFCT is the sensor (Z_{trans}=4.3 V/A).

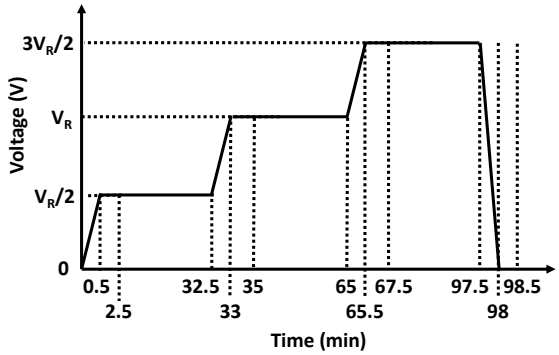

Figure 5. Ramp test profile for DC testing. V_R is the peak value of the AC PD inception voltage.

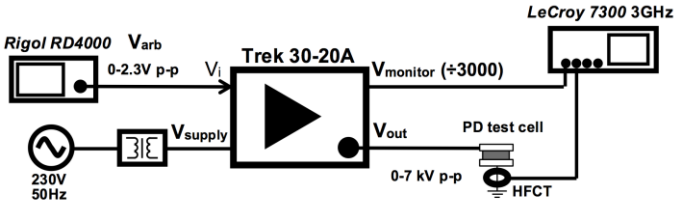

Figure 6. Diagram of experimental setup for measuring PD characteristics under HVDC and HVDC with superimposed harmonic ripple.

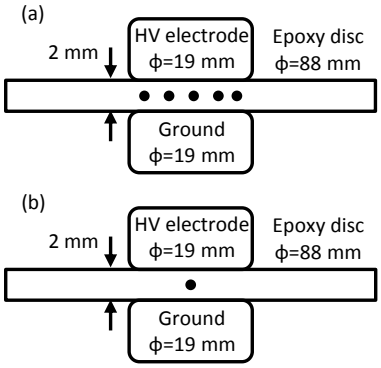

Figure 7. Dielectric samples used in (a) pure HVDC tests; five voids in epoxy resin of diameters 0.59, 0.46, 0.43, 0.32 and 0.21 mm respectively (not to scale) and (b) HVDC ripple tests; single spherical void in epoxy resin of diameter 0.6 mm.

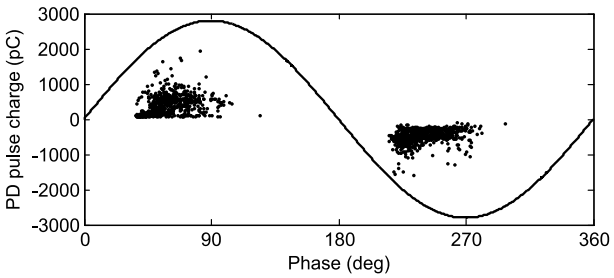

Figure 8. PRPD plot for the five void sample for 10 seconds of PD activity at 8 kV (rms).

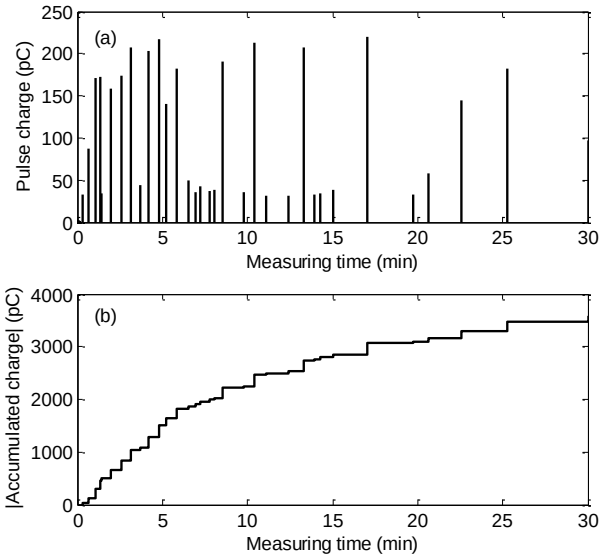

Figure 9. Five void sample. (a) Consecutive charge pulses recorded at 20 kV in 30 mins (b) Accumulated pulse charges recorded over the 30 min test period.

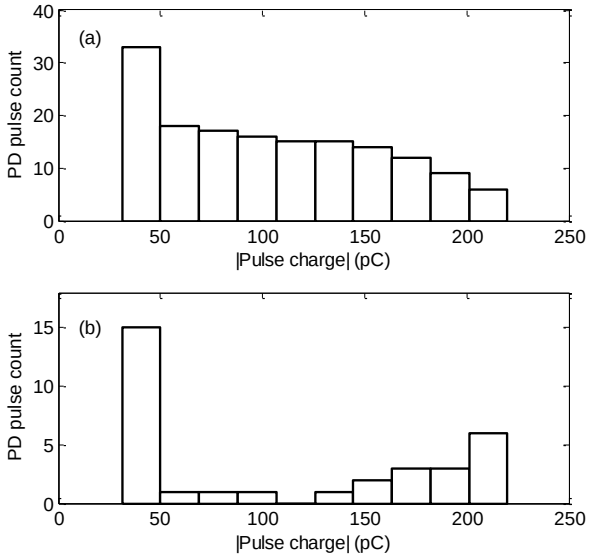

Figure 10. Five void sample. (a) Exceeding frequencies of PD pulses - the number of pulses whose apparent charge exceeds a specified threshold level (b) Class frequencies of PD pulses - total number of PD pulses whose charge lies within a defined set of ranges.

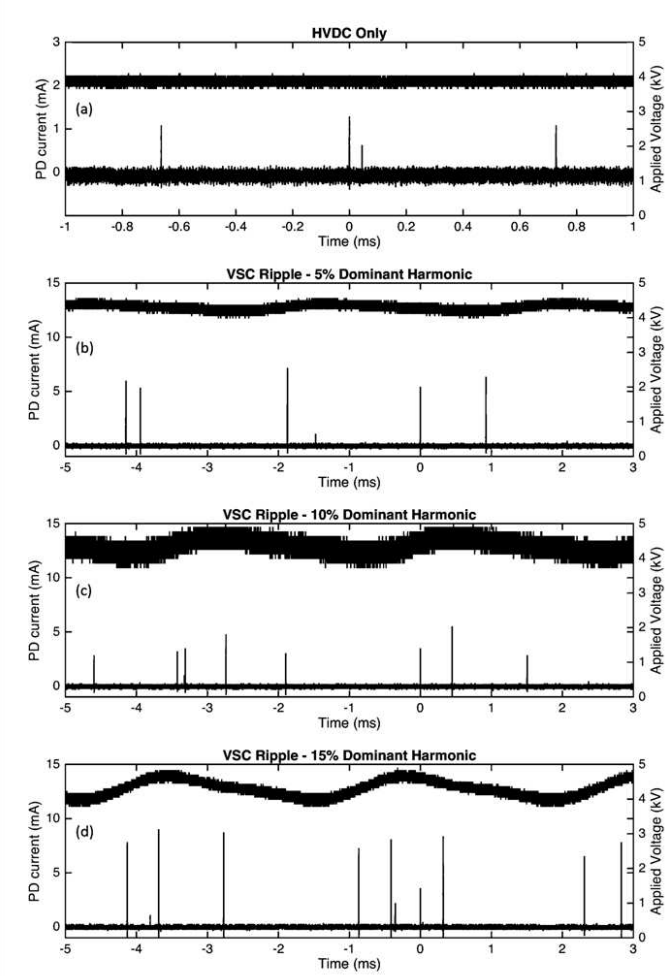

Figure 11. PD pulse characteristics on a millisecond time-scale for VSC dominant harmonic contributions of: (a) 0% (b) 5% (c) 10% (d) 15% PD was generated by a 0.6 mm void sample in solid dielectric insulation.

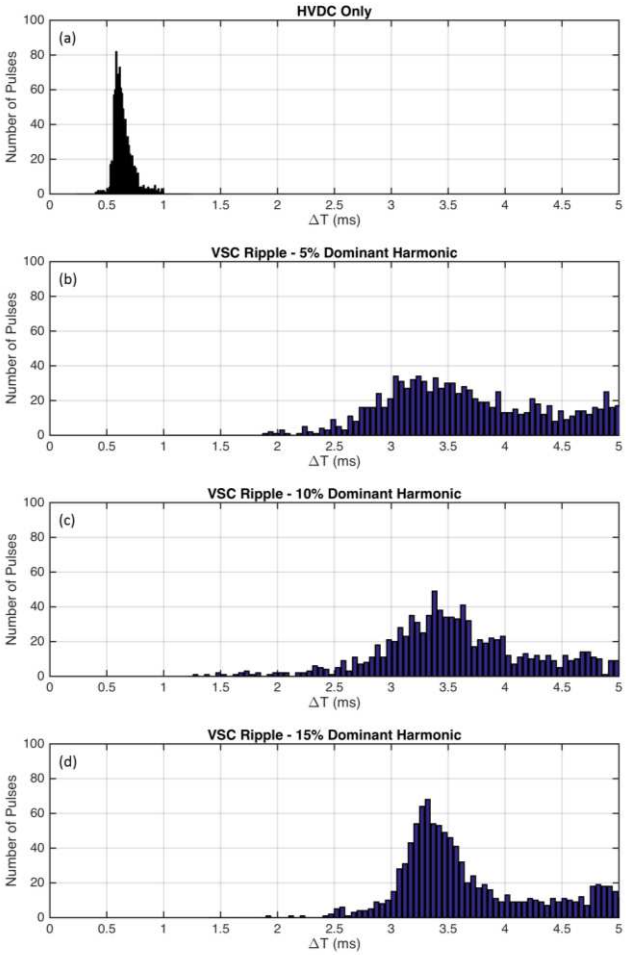

Figure 12. Distribution of PD pulse spacing for: (a) 0% (b) 5% (c) 10% (d) 15% 6^{th} harmonic relative amplitudes. PD was generated from a spherical void sample.

Tables:

Table I. Theoretical harmonic content of a 6-pulse VSC converter's voltage output

Harmonic order	Harmonic Frequency	Amplitude relative to DC
6th	300 Hz	0.0404
12th	600 Hz	0.0099