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A 1.8-3.2 GHz Doherty Power Amplifier in quasi-MMIC Technology

Roberto Quaglia, *Member, IEEE*, Mark D. Greene, Matthew J. Poulton, and Steve C. Cripps, *Life Fellow, IEEE*

Abstract—This letter presents the design and characterization of a quasi-integrated Doherty power amplifier for base-station applications. The prototype is based on GaN on SiC 0.25 μm 50 V transistors, while the passive matching networks are realized on a GaAs substrate. The design, based on a dual-input Doherty architecture, achieves a CW output power higher than 42 dBm and a back-off efficiency higher than 38% over the 1.8-3.2 GHz frequency band. By using an off-chip coupler, single input operation is also possible with a slight reduction in performance, i.e., CW output power and back-off efficiency higher than 41.4 dBm and 36%, respectively, on the 1.8-3.2 GHz band. System level characterization shows higher peak power achievable than in CW condition as well as the linearizeability of the amplifier under modulated signal conditions.

Index Terms—Wideband microwave amplifiers, broadband matching networks, GaN-based FETs.

I. INTRODUCTION

The Doherty power amplifier (DPA) [1] is widely adopted in base-stations to improve the average efficiency of high frequency transmitters in presence of modulated signals with large peak to average power ratio (PAPR). To design base-station transmitters that are easily reconfigurable in frequency, DPAs able to cover multiple bands are desirable, thus driving a great research effort in broadband DPAs [2]. Miniaturization is another important aspect of DPA development, and several recent contributions have used GaN-based integrated solutions for DPA design [3]–[10]. An interesting approach to minimize the usage of expensive SiC substrate, preferred for integrating the GaN transistors for lattice match and thermal reasons, consists of integrating the passive matching networks on a cheaper substrate, such as GaAs, and then using bond wires to interconnect the several dies, in a solution known as quasi-integrated or quasi-MMIC. A previous work by the same authors [9] has exploited a quasi-MMIC solution to design a broadband DPA based on independent inputs for main and auxiliary devices [9]. Compared to that work, this letter uses a different and improved combiner network that allows to enhance the bandwidth. Moreover, the new design is also compatible with single input operation by inserting an off-the-shelf external surface mount coupler, with an acceptable reduction in performance.

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R. Quaglia and S. Cripps are with the Centre for High Frequency Engineering, Cardiff University, Cardiff, CF24 3AA, UK. e-mail: quagliar@cardiff.ac.uk

M. Greene and M. Poulton are with Qorvo Inc., Richardson, TX 75080, USA

II. DESIGN AND SIMULATION

The output combiner of the DPA, whose function is to guarantee the correct load modulation at the intrinsic generator planes of the devices, has been designed with lumped circuit elements to allow integration. While on-chip capacitors can provide a wide range of values with low losses, spiral inductors' losses can prevent significantly the power and efficiency performance of the final DPA. As explored in [9], using a high-pass prototype for the output combiner helps minimizing the number of high value inductors thus reducing losses. In the proposed topology, the auxiliary drain bias is around two times the main's one, in order to accommodate the higher voltage swing [11]. This leads to a reduction of the power utilisation factor of the active devices, but helps maintaining good back-off efficiency over a large bandwidth. The design is based on Qorvo's AlGaIn/GaN HEMT 0.25 μm high voltage technology, on SiC substrate. Targeting a maximum output power around 25 W, the devices selected are a 6x350 μm for the main and a 6x400 μm for the auxiliary. The passive matching network are synthesised on the Qorvo's IPC3 passive component process, on GaAs substrate. To increase the bandwidth compare to

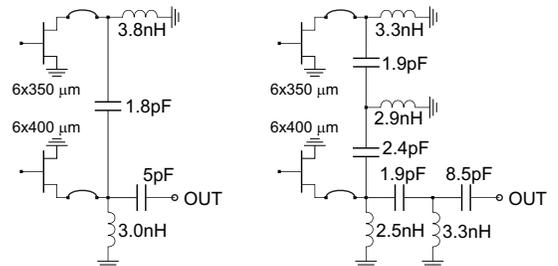


Fig. 1. Scheme diagram of the q-MMIC DPA output. Left: old design presented in [9]; Right: new design presented in this paper.

previous designs, and in particular to [9], the DPA proposed here uses a 2-stage high-pass filter to connect the main and auxiliary outputs with an impedance inverter equivalent behaviour, while an additional output matching is adopted to improve the matching of the auxiliary at saturation, see the two schematics of the output combiners in Fig. 1. The design is supported by the foundry large signal model of the device. The lumped components values are adjusted to absorb the devices' capacitance and the bond wires effects, while the splitting ratio between the main and auxiliary inputs is considered as an additional degree of freedom during the design. Simulations show that, for the splitting ratio, a linear

phase vs. frequency behaviour leads to a marginal performance reduction compared to the fully optimised profile. On the other hand, the amplitude needs to be adjusted at each frequency and drive level. The input matching networks include broadband

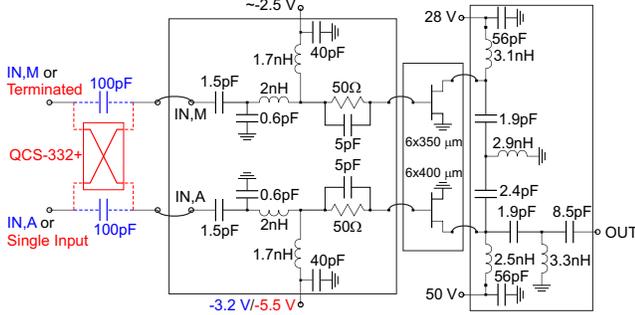


Fig. 2. Scheme diagram of the q-MMIC DPA. Notations in blue or red refer to dual- or single-input, respectively.

stabilization. Fig. 2 shows the complete schematic of the DPA, including the input board that can be used for dual- or single-input operation when mounting off-chip capacitors or a coupler (QCS-332+ from MiniCircuits), respectively. The losses of the critical drain inductors are minimized by employing bond-wires to extract the centre tap. Fig. 3 compares the simulated load trajectories of this new design with the ones from [9].

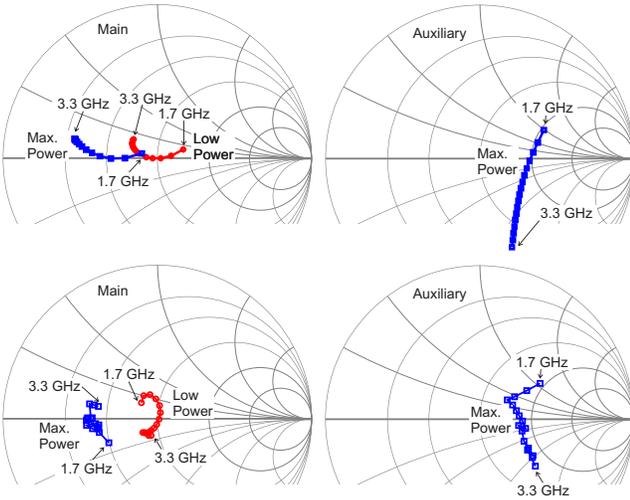


Fig. 3. Simulated load trajectories ($Z_0 = 50\Omega$) at intrinsic generator planes (red and blue). Top: design of [9]. Bottom: the proposed new design.

Fig. 4 summarizes the simulated results of the DPA. The relative phase between auxiliary and main input varies linearly between 107° at 1.7 GHz and 88° at 3.3 GHz, remaining quite close to 90° across the band. This means that the hybrid coupler can provide a reasonable, although sub-optimal, solution to simplify the utilization of this DPA.

III. EXPERIMENTAL CHARACTERIZATION

The fabricated and assembled DPA, whose pictures are shown in Fig. 5, has been characterized in CW with single-tone and modulated signal stimulus, from 1.7 GHz to 3.3 GHz,

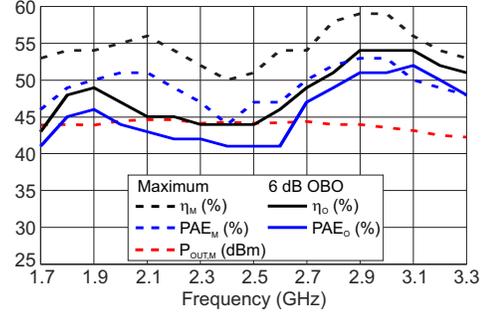
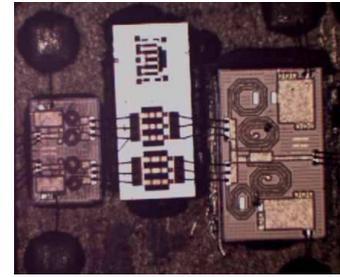
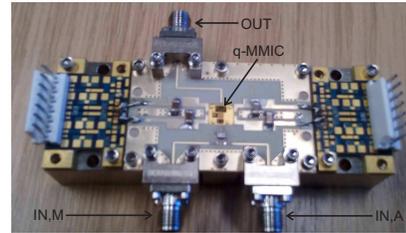


Fig. 4. Simulated CW single tone output power, efficiency and PAE at maximum power (dashed) and 6 dB back-off (solid).

with 50 MHz step. Fig. 6 shows the CW efficiency and gain



(a)



(b)

Fig. 5. (a) Microscope picture of the q-MMIC assembly (total size 4.8 mm x 2.9 mm). (b) Picture of the fabricated test fixture.

vs. output power at some frequencies for the DPA operating in dual-input configuration. The ratio between the inputs is adjusted at each frequency for best back-off efficiency while maintaining a reasonably flat gain response vs. power. The gain already includes the total input power. Fig. 7 summarizes the CW performance vs. frequency for both dual- and single-input operation. Compared to simulations, there is a decrease in performance in the higher part of the band.

For dual-input, the output power is higher than 42 dBm and the back-off efficiency is higher than 38% over the 1.8-3.2 GHz frequency band. With single input, the output power and back-off efficiency are higher than 41.4 dBm and 36%, respectively, on the 1.8-3.2 GHz band. The reduction in output power is due both to sub-optimal phase adjustment and deeper class C bias of the auxiliary gate to avoid early turn-on. Table I compares the measured results in the two cases with the state of the art of integrated DPAs. There is a clear improvement compared to [9], with increase in bandwidth

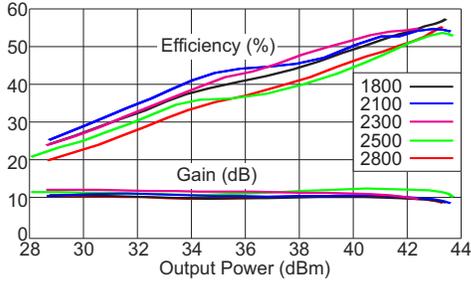


Fig. 6. Measured CW efficiency and gain vs. output power, at some frequencies, in dual input operation.

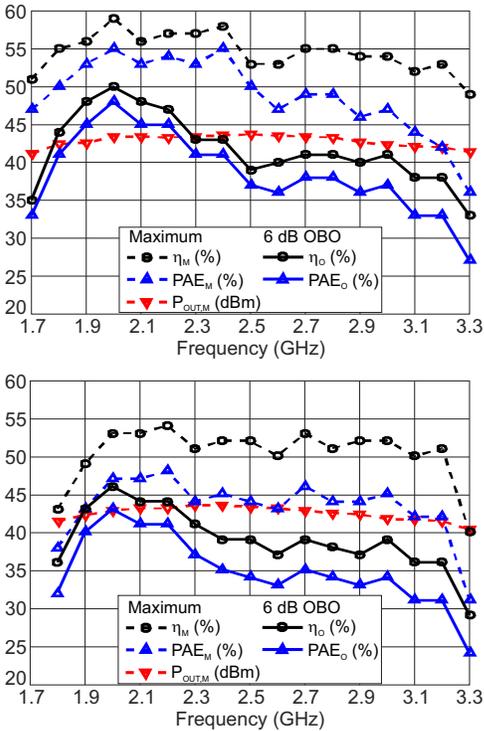


Fig. 7. Measured CW results vs. frequency. Dual input (top); Single input (bottom).

(1 GHz to 1.5 GHz) and output power (40.2 dBm to 42 dBm). System level characterization has been performed with a LTE signal with 9 dB PAPR and 20 MHz channel. On the whole band, the achievable maximum power is 1-1.5 dB higher than with single tone due to relaxed thermal effects. Fig. 8 reports the output spectra without and with digital predistortion, at 1.9 GHz (left) and 2.8 GHz (right), in the single-input case, that is more critical for linearity since the amplitude and phase distortion profiles are less controllable. The native Adjacent Channel Leakage Ratio (ACLR) is rather good (≈ -30 dBc), and the adoption of predistortion brings the ACLR below -49 dBc.

IV. CONCLUSIONS

A quasi-integrated Doherty power amplifier in GaN technology that can operate with dual- or single-input has been

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED DOHERTY PA ICs.

Ref.	Freq. (GHz)	$P_{OUT,MAX}$ (dBm)	η_{SAT} (%)	η_{OBO} (%)	OBO (dB)	Gain (dB)
[3]	2.14	40.5	60	52	7.1	16
[4]	2.14	41.2	57	43	4.7	20
[5]	0.75–0.77	39	46	37	7.2	46
[6]	2.1–2.7	41	n.a.	46	7.2	12
[7]	2.655	42.2	n.a.	47	7.1	31
[8]	2.6	45	n.a.	45	6	28
[9]	1.7–2.7	40.2	42	37	6	12
[10]	2.6	44	63	52	6.5	18
D.I.	1.8–3.2	42.0	52	38	6	9
S.I.	1.8–3.2	41.4	43	36	6	9

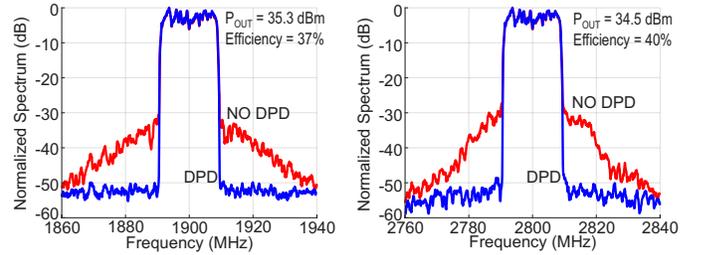


Fig. 8. Measured spectra with LTE signal (20 MHz channel, 9 dB PAPR), single input. Without predistortion: red; With Predistortion: blue.

presented. The CW single-tone measured results compare well with the state-of-the-art, while modulated signal measurements demonstrate the linearizability of the hardware.

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