A SiC-based Neutral Leg for the Three-phase Four-wire Inverter

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***Abstract*—SiC-based inverters can operate at high switching frequency with high efficiency, which can reduce the size of passive components and heat sinks to achieve high power density. However, in three-phase four-wire inverters supplying unblanced loads, the second-order ripples in the DC bus need to be mitigated by large DC capacitance, which increases the size of the converter. The conventional neutral leg is widely used in three-phase four-wire inverters to provide neutral currents for the unbalanced loads. In this paper, an improved neutral leg is proposed, which can provide neutral currents and reduce the second-order ripples in the DC bus simultaneously. The DC bus ripples can be reduced without adding any hardware components. Furthermore, the proposed neutral leg can save 50% DC capacitance comparing to the conventional neutral leg. The proposed neutral leg was built with SiC MOSFETs and tested with a three-phase four-wire inverter in the laboratory. The experimental results verified the effectiveness of the proposed neutral leg.**

***Index Terms*—Neutral leg; three-phase four-wire inverter; second-order power ripple; SiC MOSFET; unbalanced loads.**

I. Introduction

In smart grids, three-phase inverters have been widely used as an interface between the active distribution network (ADN) and the distributed energy resources (DER) [1], such as solar PVs, wind turbines and energy storage systems. Another new trend in smart grid and traction systems is to replace the conventional bulky transformers with more compact solid-state transformers (SST), which also require three-phase inverters to feed the loads [2]. When the DERs and SSTs are used to supply unblanced loads or connected to an unbalanced grid, the three-phase four-wire inverters are usually required to provide the additional path for the zero-sequence current of the loads, i.e. the neutral current [3].

There are various topologies of three-phase four-wire inverters [4]. One of the popular topologies is the three-phase inverter with an independently-controlled neutral leg as shown in Fig. 1a [5]. In this topology, a neutral leg is connected to the midpoint of the split capacitors in the DC bus through a neutral inductor. In this way, the neutral current can be provided by the neutral leg with active control. Additionally, the voltages of the split capacitors can be balanced by the neutral leg. Moreover, this topology also allows the independent control of the neutral leg and avoids EMI problems [6].

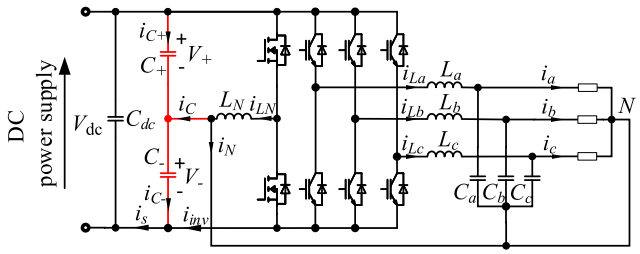
As the emerging wide bandgap (WBG) semiconductor devices, SiC MOSFETs feature high breakdown electric field, low on-resistance, fast switching speed, and high junction temperature capability [7]. These characteristics allows the SiC MOSFET to operate at higher switching frequency with low power losses comparing to its Si counterparts, which results in reduced size of passive components and heat sinks. Therefore, higher power density can be achieved by SiC MOSFETs.

In three-phase four-wire system with unbalanced loads, besides the challenge of providing neutral currents, another challenge is the second-order current and voltage ripples in the DC bus caused by the unbalanced loads [8] . Although SiC MOSFETs can reduce the size of passive components such as the filter inductors and filter capacitors, the large capacitance is still required by the DC bus to mitigate the second-order ripples, which becomes the bottleneck to achieve high power density.

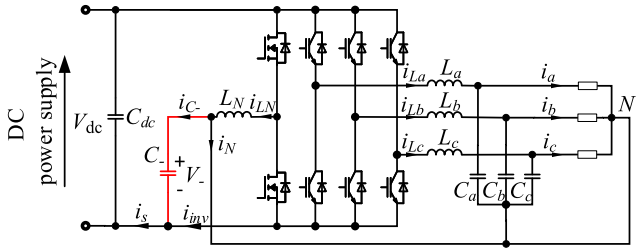
When the topology with the conventional neutral leg is used, large DC capacitance is required to mitigate the second-order ripples. Also, the DC-bus ripples cannot be fully eliminated so that no loads/sources can be directly connected to the DC-bus. Although there are many active power decoupling solutions to reduce both the ripples and capacitance in the DC bus [9], these solutions require extra switches and passive components, which increases the cost of the converter.

In this paper, an improved neutral leg is proposed, which can address the aforementioned two challenges in three-phase four-wire inverters with unbalanced loads simultaneously: a) to provide neutral currents; b) to reduce second-order ripples in the DC bus. Since the DC-bus ripples are reduced, the proposed neutral leg can save 50% capacitance comparing to the conventional neutral leg, which can reduce the size of the converter.

The rest of this paper is organized as follows. In Section II, the second-order ripples in the DC bus are analyzed. After that, the proposed neutral leg and its operation principles are presented in Section III. Then, Section IV illustrates the control strategy of the three-phase four-wire inverter with the proposed neutral leg. In Section V, the proposed neutral leg is compared with the conventional neutral leg in terms of DC capacitance. In Section VI, the proposed neutral leg is built with SiC MOSFETs and tested with the three-phase inverter. The experimental results are given to verify the effectiveness of the proposed neutral leg. Finally, conclusions are made in Section VII.



(a) With the conventional neutral leg.



(b) With the proposed neutral leg by removing C_+.

Figure 1. Three-phase four-wire inverter with neutral legs.

II. DC-bus Ripples for Three-phase Four-wire Inverters

For three-phase four-wire inverters supplying unbalanced loads, the instantaneous output power on the AC side can be calculated as [10]:

$$p_{ac} = P_o + p_{2\omega} = P_o + P_{2\omega}\cos\left(2\omega t + \phi\right) \tag{1}$$

where P_o is the average value of the output power; $P_{2\omega}$ and ϕ are the amplitude and phase angle of the second-order power ripple $p_{2\omega}$ respectively. Assuming the three-phase voltages are balanced, the second-order power ripple is caused by the negative-sequence component of the unbalanced three-phase currents [8]. The unbalance factor can be defined as:

$$\delta = \frac{I^-}{I^+} = \frac{P_{2\omega}}{P_o} \tag{2}$$

where I^+ and I^- are the rms values of the positive- and negative- sequence currents.

Due to the power balance between AC side and DC side, the second-order power ripple will inevitably propagate to the DC side. This leads to second-order ripples in either DC-bus voltage or current. It is often required to limit such ripples because they can deteriorate system performance [11]. For example, second-order ripples make it hard to achieve Maximum Power Point Tracking (MPPT) for single-stage solar PV systems because the maximum power point depends on the DC output voltage of the PV panels [12]; Second-order ripples might reduce the lifetime and performance of batteries [13] and fuel cells [14]; Large second-order ripples might cause the maximum DC-bus voltage exceeding the safety margin of the semiconductors; Large DC ripples might affect the power quality of three-phase ouput voltages/currents [15], which need to be compensated by the controller of the three-phase inverter.

The main contribution of this paper is to propose a solution for three-phase four-wire inverters which can achieve three objectives:

1) Reduced DC-bus ripples;
2) Reduced DC capacitance;
3) No additional components required.

To achieve these three objectives, an improved neutral leg is proposed to reduce the DC-bus ripples while providing the neutral current for the loads.

III. The Proposed Neutral Leg

The proposed neutral leg is shown in Fig. 1b. Comparing to the conventional one in Fig. 1a, the proposed neutral leg removes the upper capacitor C_+ from the DC bus. Although the modification seems minor, it actually enables the proposed neutral leg to reduce second-order ripples in the DC bus and accordingly reduce the required capacitance. By removing C_+, the second-order power ripple can be transferred from the DC bus to C_-. Importantly, the proposed neutral leg can still achieve the function of the conventional neutral leg, i.e., supplying neutral currents.

A. Reducing DC-bus Ripples

To reduce the second-order ripples in the DC bus, the proposed neutral leg can work as an active energy storage circuit to transfer the second-order power ripple from the DC bus to C_- by applying a second-order voltage component to C_- with an offset of half the DC-bus voltage $V_{dc}/2$:

$$v_-\left(t\right) = \frac{V_{dc}}{2} + V_{C\_2\omega}\sin\left(2\omega t + \theta_{2\omega}\right) \tag{3}$$

where $V_{C\_2\omega}$ and $\theta_{2\omega}$ are the amplitude and phase angle of the second-order component respectively. The instantaneous power p_{C-} provided by C_- can be calculated as:

$$\begin{aligned} p_{C-} &= v_-\left(t\right) C_N \frac{dV_-}{dt} = p_{C-\_2\omega} + p_{C-\_4\omega} \\ &= \omega C_N V_{C\_2\omega} V_{dc}\cos\left(2\omega t + \theta_{2\omega}\right) \\ &+ \omega C_N V_{C\_2\omega}^2 \sin\left(4\omega t + 2\theta_{2\omega}\right). \end{aligned} \tag{4}$$

In this case, if the instantaneous power of the neutral inductor L_N is neglected, the second-order power ripple on the DC bus can be compensated by the proposed neutral leg if $p_{C-\_2\omega}$ in (4) is equal to $p_{2\omega}$ in (1). Therefore, $V_{C\_2\omega}$ and $\theta_{2\omega}$ can be calculated as:

$$V_{C\_2\omega} = \frac{P_{2\omega}}{\omega C_N V_{dc}} \tag{5}$$

$$\theta_{2\omega} = \phi. \tag{6}$$

B. Supplying the Neutral Current

The proposed neutral leg has the same capability as the conventional neutral leg to provide the neutral current to unbalanced loads. The current provided by the neutral inductor L_N consists of two parts:

$$i_{L_N} = i_N + i_{C-} \tag{7}$$

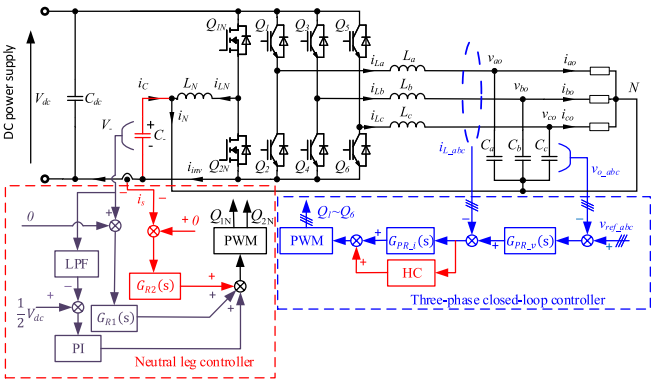


Figure 2. Proposed control diagram.

where i_N is the neutral current required by the unbalanced loads; i_{C-} is the compensation current injected to C_- to reduce second-order ripples in the DC bus. Two independent controllers can be adopted to control i_N and i_{C-} respectively so that the proposed neutral leg can still provide the neutral current required by the loads. The control strategy is proposed in the next section.

IV. Control Design

The control strategy for the three-phase four-wire inverter with the proposed neutral leg is shown in Fig. 2, which consists of two parts. The first part is the control of the proposed neutral leg. The second part is the closed-loop control of the three-phase four-wire inverter. These two parts can work independently. Comparing to the conventional neutral leg, the proposed neutral leg only requires two additional controllers: one is the power decoupling controller $G_{R2}(s)$ to decouple the second-order ripples from the DC bus; the other one is the harmonic compensator (HC) added in the current loop of the three-phase inverter to compensate the harmonics in load currents.

A. Control of the Proposed Neutral Leg

The control of the proposed neutral leg consists of the neutral current controller and the power decoupling controller.

1) Neutral Current Controller : The neutral current controller of the proposed neutral leg works the same as the neutral current controller of the conventional neutral leg. Therefore, the same controller for the conventional neutral leg can be directly adopted by the proposed neutral leg. Since the neutral current control strategy is not the main focus of this paper, a simple PI controller in parallel with a resonant controller is applied with the assumption that the neutral current only contains the fundamental component.

Firstly, the average voltage of C_- is controlled to be half the DC-bus voltage $V_{dc}/2$ to maintain the neutral point voltage of the AC system. In order to get the average voltage of C_-, a low-pass filter (LPF) is adopted to extract the DC component of V_-:

$$LPF(s) = \frac{\omega_c}{s+\omega_c} \tag{8}$$

where ω_c is the cut-off frequency of the LPF. To filter out the harmonic components at 100 Hz and beyond, ω_c is set as 50 rad/s. A proportional-integral (PI) controller can be applied to regulate the average value of V_- to be $V_{dc}/2$:

$$PI(s) = k_p + \frac{k_i}{s} \tag{9}$$

where k_p and k_i are the proportional gain and integral gain of the PI controller respectively.

Secondly, to ensure that the neutral current is mainly provided through the neutral inductor L_N instead of the capacitor C_-, a resonant controller $G_{R1}(s)$ is applied:

$$G_{R1}(s) = \frac{2\xi_1 \omega s}{s^2 + 2\xi_1 \omega s + \omega^2} \times K_{R1} \tag{10}$$

where ω is the fundamental angular frequency; ξ_1 defines the cut-off frequency of the resonant controller; K_{R1} is the resonant gain of the controller. The gain of $G_{R1}(s)$ is almost zero everywhere apart from the resonant frequency ω. V_- can be measured as the feedback of $G_{R1}(s)$ to regulate its fundamental component to be zero.

2) Power Decoupling Controller: In the power decoupling controller, another resonant controller $G_{R2}(s)$ is applied:

$$G_{R2}(s) = \frac{2\xi_2 (2\omega) s}{s^2 + 2\xi_2 (2\omega) s + (2\omega)^2} \times K_{R2} \tag{11}$$

where ξ_2 defines the cut-off frequency; K_{R2} is the resonant gain of the controller. $G_{R2}(s)$ has the resonant peak at 100 Hz. With the DC-bus current i_s as the feedback of $G_{R2}(s)$, the second-order components of i_s can be controlled to be zero.

With the neutral current controller and the power decoupling controller paralleled together, the proposed neutral leg can provide neutral currents and reduce DC-bus ripples simultaneously.

B. Control of the Three-phase Inverters

In this paper, the three-phase four-wire inverter works in standalone mode to supply the unbalanced loads with balanced three-phase voltages. Therefore, AC voltage closed-loop control is performed with inner current loop. The three phases are independently controlled by proportional-resonant (PR) current and voltage controllers:

$$G_{PR\_v}(s) = K_{p\_v} + \frac{2\xi_v \omega s}{s^2 + 2\xi_v \omega s + \omega^2} \times K_{R\_v} \tag{12}$$

$$G_{PR\_i}(s) = K_{p\_i} + \frac{2\xi_i \omega s}{s^2 + 2\xi_i \omega s + \omega^2} \times K_{R\_i} \tag{13}$$

where K_{p_v} and K_{p_i} are the proportional gains of the voltage and current controller respectively; K_{R_v} and K_{R_i} are the resonant gains of the voltage and current controllers respectively; ξ_v and ξ_i are the coefficients of cut-off frequency. In addition, the second-order harmonics need to be compensated by the current controller due to the voltage variation of the neutral point caused by the power decoupling controller $G_{R2}(s)$. Therefore, as shown in Fig. 2, a harmonic

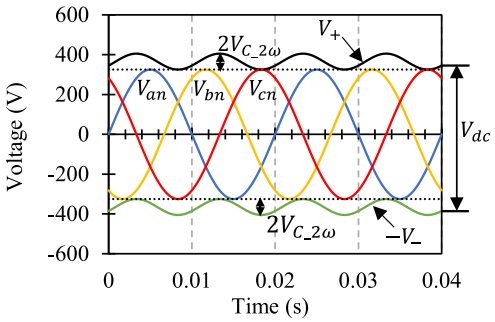


Figure 3. Minimum DC voltage requirement of the proposed neutral leg.

compensator (HC) is in parallel with $G_{PR\_i}(s)$ to compensate the current harmonics at 100 Hz:

$$HC(s) = \frac{2\xi_{HC}(2\omega)s}{s^2 + 2\xi_{HC}(2\omega)s + (2\omega)^2} \times K_{HC}. \quad (14)$$

where ξ_{HC} defines the cut-off frequency of $HC(s)$; K_{HC} is the resonant gain of the controller.

V. Comparisons of DC-bus Capacitance

In this section, the proposed neutral leg is compared with the conventional neutral leg in terms of DC-bus capacitance under the assumption of the same maximum DC-bus voltage. To make the comparison, the DC-bus voltage requirement of each solution is first analyzed.

A. DC-bus Voltage Requirement

In three-phase four-wire inverters with neutral legs, the following equation should be fullfilled to produce balanced three-phase voltages [6]:

$$\begin{cases} v_+(t) \geq \sqrt{2}V_{rms} \\ v_-(t) \geq \sqrt{2}V_{rms} \end{cases} \quad (15)$$

where V_{rms} is the rms value of phase-to-ground voltages. Under the balanced condition, since there are no second-order ripples in the DC bus, the minimum DC-bus voltage can be achieved:

$$V_{dc\_min} = 2\sqrt{2}V_{rms} \quad (16)$$

For the proposed neutral leg with power decoupling control, although there is no voltage ripples on V_{dc}, both V_+ and V_- contain voltage ripples because the second-order ripples from the DC bus are absorbed by C_-. Substituting (3) into (15) results in:

$$\frac{V_{dc}}{2} + V_{C\_2\omega}\sin(2\omega t + \theta_{2\omega}) \geq \sqrt{2}V_{rms}. \quad (17)$$

Therefore, as shown in Fig. 3, the total DC-bus voltage required by the proposed neutral leg is

$$V_{dc} \geq 2\sqrt{2}V_{rms} + 2V_{C\_2\omega}. \quad (18)$$

Substituting (2) and (5) into (18) results in:

$$V_{dc} \geq 2\sqrt{2}V_{rms} + \frac{2\delta P_0}{\omega C_- V_{dc}} \quad (19)$$

The DC-bus voltage required by the proposed neutral leg can be obtained by solving (19):

$$V_{dc,pro} \geq \sqrt{2}V_{rms} + \sqrt{2V_{rms}^2 + \frac{2\delta P_0}{\omega C_-}}. \quad (20)$$

For the conventional neutral leg, since V_+ and V_- are balanced controlled to be half the DC-bus voltage, the total DC-bus voltage required should be

$$v_{dc,con}(t) \geq 2\sqrt{2}V_{rms}. \quad (21)$$

With the conventional neutral leg, the unbalanced AC load will cause second-order voltage ripples on the DC bus, the DC bus voltage and the amplitude of the second-order voltage ripple can be calculated according to [8]:

$$v_{dc,con}(t) = V_{dc\_avg,con} + V_{dc\_2\omega,con}\sin(2\omega t + \theta) \quad (22)$$

$$V_{dc\_2\omega,con} = \frac{\delta P_0}{2\omega C_{eq} V_{dc\_avg,con}} \quad (23)$$

where $V_{dc\_avg,con}$ is the average DC-bus voltage. $V_{dc\_2\omega,con}$ is the amplitude of the second-order voltage ripple in the DC bus; C_{eq} is the equvalent DC-bus capacitance. The average and maximum DC-bus voltages can be obtained according to (21), (22) and (23):

$$V_{dc\_avg,con} \geq \sqrt{2}V_{rms} + \sqrt{2V_{rms}^2 + \frac{\delta P_0}{2\omega C_{eq}}} \quad (24)$$

$$V_{dc\_max,con} \geq \sqrt{8V_{rms}^2 + \frac{2\delta P_0}{\omega C_{eq}}} \quad (25)$$

where $V_{dc\_max,con} = V_{dc\_avg,con} + V_{dc\_2\omega,con}$, which is the maximum DC-bus voltage caused by unbalanced second-order power ripple with the conventional neutral leg.

B. DC Capacitance

Normally, 1200 V semiconductor switches (Si-IGBTs or SiC-MOSFETs) are selected for three-phase inverters supplying AC voltages of 230 Vrms. Therefore, the DC-bus voltage should not exceed 1200 V. Besides, the higher DC-bus voltage results in higher voltage stresses to the switches, which will increase the switching losses. Therefore, considering the voltage stresses and safe margin for the voltage overshoot of switches, the maximum DC-bus voltage V_{max} is selected to be 750 V for comparison in this paper. The DC-bus capacitance should be designed to make sure the DC-bus voltage doesn't exceed 750 V.

In Fig. 1, C_{dc} is the sum of small film capacitors which are placed closed to the switches to reduce voltage overshoot and switching harmonics. The value of C_{dc} is less than 10 μF so it is negligible. The major part of the DC-bus capacitance is the capacitance of the neutral legs. The capacitors rated at 450 V are usually connected in series to support the 750 V DC-bus voltage. However, the equivalent DC-bus capacitance reduces due to the series connection of capacitors.

In the conventional neutral leg, two capacitors C_+ and C_- are used in the DC bus. Considering C_+ and C_- are equal, the equivalent DC-bus capacitance is:

$$C_{eq} = \frac{1}{2}C_+ = \frac{1}{2}C_- \tag{26}$$

and the total capacitance is

$$C_{total} = 2C_+ = 4C_{eq}. \tag{27}$$

In the proposed neutral leg, since only one capacitor C_- is used, the total capacitance of the proposed neutral leg is

$$C_{total} = C_- \tag{28}$$

According to (20) and (25), the required total capacitance of all the solutions can be calculated according to the maximum DC-bus voltage V_{max}:

$$C_{total,pro} \geq \frac{2\delta P_0}{\omega\left(V_{max} - 2\sqrt{2}V_{rms}\right)} \cdot \frac{1}{V_{max}} \tag{29}$$

$$C_{total,con} \geq \frac{2\delta P_0}{\omega\left(V_{max} - 2\sqrt{2}V_{rms}\right)} \cdot \frac{4}{\left(V_{max} + 2\sqrt{2}V_{rms}\right)} \tag{30}$$

where $C_{total,pro}$ and $C_{total,con}$ are the values of the total capacitance required by the proposed and conventional neutral legs respectively. The following relations can be obtained from the above equations:

$$\frac{C_{total,pro}}{C_{total,con}} = \frac{\left(V_{max} + 2\sqrt{2}V_{rms}\right)}{4V_{max}} < \frac{1}{2} \tag{31}$$

According to (31), comparing to the conventional neutral leg, the proposed neutral leg can reduce the total DC-bus capacitance by at least 50%. The capacitance requirements of the proposed and conventional neutral legs are compared in Fig. 4. The maximum DC-bus voltage is set as 750 V. The unbalance factor is 0.5. Comparing to the conventional neutral leg, the proposed one only requires less than 50% capacitance to fullfill the same maximum DC-bus voltage requirement.

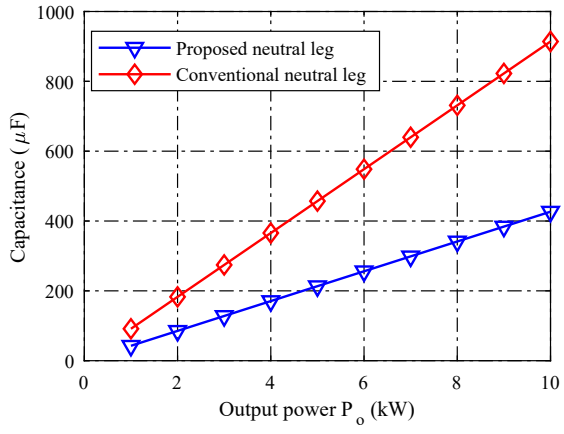


Figure 4. Comparison of total DC capacitance (V_{dc}=750 V, $\delta = 0.5$).

Table I
EXPERIMENTAL PARAMETERS.

DC voltage	360 V	AC output voltage	110 Vrms
AC Filter inductor	2.5 mH	AC filter capacitor	20 μF
Neutral inductor L_N	2.5 mH	Neutral capacitor C_-	100 μF
Unbalanced loads	$R_a = 52\,\Omega, R_b = R_c = 210\,\Omega$		

VI. EXPERIMENTAL RESULTS

Experimental platform was built to verify the proposed topology. The proposed neutral leg was built with SiC MOSFETs (C2M0080120D) and SiC diodes (C4D20120D). It was controlled by dSPACE with the switching frequency at 50 kHz. The three-phase inverter was built with Si IGBTs (MMIX1Y100N120C3H1) and controlled by DSP+FPGA with the switching frequency at 20 kHz. The experimental parameters were summarized in Table I. The DC-bus voltage is supplied by a DC voltage source, so the DC-bus voltage is constant and only the second-order current ripple exists in the DC bus. The proposed neutral leg was verified in the experiment by reducing the second-order current ripple in the DC bus. Firstly, only the neutral current controller in Fig. 2 was applied to the proposed neutral leg. In this case, the proposed neutral leg worked the same as the conventional neutral leg. As is shown in Fig. 5, the load voltages were balanced controlled and the load currents were unbalanced due to unbalanced loads. It can be seen that the neutral current I_N was provided by the neutral inductor L_N instead of the capacitor C_- because there was nearly no 50 Hz ripples in V_-. Also, the DC source current I_{dc} contained large second-order harmonics due to the unbalanced load currents as shown in Fig. 5 and Fig. 7.

Secondly, the power decoupling controller in Fig. 2 was applied to the proposed neutral leg in parallel with the neutral current controller. As shown in Fig. 6, the DC source current ripples were significantly reduced. In Fig. 7, the FFT analysis of the DC source current is shown. It can be seen that with the power decoupling controller, the second-order harmonics in DC source current reduced by 86%. In Fig. 6, the capacitor voltage V_- contained the second-order voltage ripple due to the power decoupling controller. However, the load voltages and currents were not affected. As shown in Fig. 8, the total THD of the load voltage of Phase C was 0.874% without power decoupling controller and 0.864% with power decoupling controller.

VII. CONCLUSIONS

This paper presented an improved SiC-based neutral leg which can provide neutral currents and reduce second-order DC bus ripples at the same time. The principle and control strategy of the proposed neutral leg is presented. Besides, comparing to the conventional neutral leg, the proposed neutral leg can reduce 50% DC-bus capacitance without adding any other active or passive components. The proposed neutral leg was built with SiC MOSFETs and tested with the three-phase inverter. The effectiveness of the proposed neutral leg was

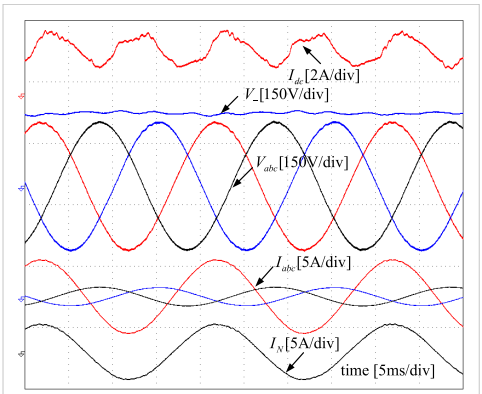


Figure 5. Experimental results of proposed neutral leg w/o power decoupling control.

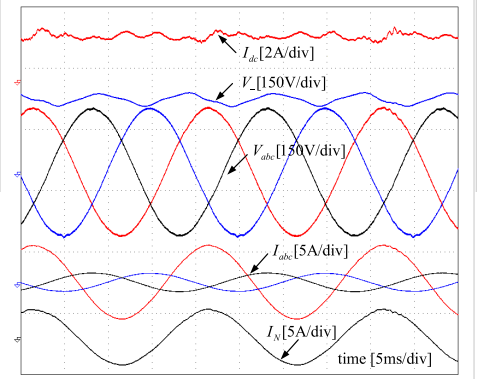


Figure 6. Experimental results of proposed neutral leg with power decoupling control.

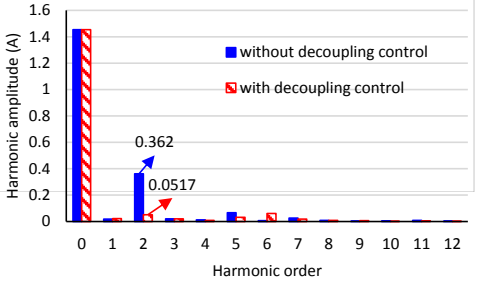


Figure 7. FFT analysis of I_{dc}.

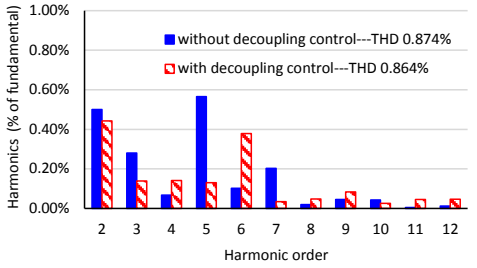


Figure 8. FFT analysis of load voltage V_a.

verified by the experimental results. The future work includes optimizing the neutral inductor of the SiC-based neutral leg and analyzing the overall efficiency.

Acknowledgement

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement no. 765585. This document reflects only the author's views; the European Commission is not responsible for any use that may be made of the information it contains.

References

[1] Q. Zhong, "Power-electronics-enabled autonomous power systems: Architecture and technical routes," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5907–5918, 2017.

[2] K. Mainali, A. Tripathi, S. Madhusoodhanan, A. Kadavelugu, D. Patel, S. Hazra, K. Hatua, and S. Bhattacharya, "A transformerless intelligent power substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electron. Mag.*, vol. 2, no. 3, pp. 31–43, 2015.

[3] Z. Lin, X. Ruan, L. Jia, W. Zhao, H. Liu, and P. Rao, "Optimized design of the neutral inductor and filter inductors in three-phase four-wire inverter with split DC-link capacitors," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 247–262, 2019.

[4] Q.-C. Zhong and T. Hornik, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. Wiley-IEEE Press, 2013.

[5] T. Hornik and Q.-C. Zhong, "Parallel PI voltage–H^∞ current controller for the neutral point of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1335–1343, 2013.

[6] J. Liang, T. C. Green, C. Feng, and G. Weiss, "Increasing voltage utilization in split-link, four-wire inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1562–1569, 2009.

[7] F. Wang, E. A. Jones, and Z. Zhang, *Characterization of wide bandgap power semiconductor devices*. Institution of Engineering & Technology, 2018.

[8] C. F. Nascimento, E. H. Watanabe, O. Diene, A. B. Dietrich, A. Goedtel, J. J. C. Gyselinck, and R. F. S. Dias, "Analysis of noncharacteristic harmonics generated by voltage-source converters operating under unbalanced voltage," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 951–961, 2017.

[9] Q. Zhong, W. Ming, W. Sheng, and Y. Zhao, "Beijing converters: Bridge converters with a capacitor added to reduce leakage currents, DC-bus voltage ripples, and total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 325–335, 2017.

[10] E. H. W. H. Akagi and M. Aredes, *Instantaneous Power Theory and Applications to Power Conditioning*. Wiley-IEEE Press, 2007.

[11] Y. Liu, B. Ge, H. Abu-Rub, and D. Sun, "Comprehensive modeling of single-phase quasi-z-source photovoltaic inverter to investigate low-frequency voltage and current ripple," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4194–4202, 2015.

[12] Y. Kuo, T. Liang, and J. Chen, "Novel maximum-power-point-tracking controller for photovoltaic energy conversion system," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 594–601, 2001.

[13] D. Patil and V. Agarwal, "Compact onboard single-phase EV battery charger with novel low-frequency ripple compensator and optimum filter design," *IEEE Trans. Veh. Technol.*, vol. 65, no. 4, pp. 1948–1956, 2016.

[14] G. Fontes, C. Turpin, S. Astier, and T. A. Meynard, "Interactions between fuel cells and power converters: Influence of current harmonics on a fuel cell stack," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 670–678, 2007.

[15] A. J. Roscoe, S. J. Finney, and G. M. Burt, "Tradeoffs between AC power quality and DC bus ripple for 3-phase 3-wire inverter-connected devices within microgrids," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 674–688, 2011.