A Four-leg Buck Inverter for Three-phase Four-wire Systems with the Function of Reducing DC-bus Ripples

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***Abstract*—Three-phase four-wire inverters are usually used to feed unbalanced three-phase loads with neutral currents. The unbalanced three-phase loads also bring to second-order ripples in the DC bus, which should be mitigated by bulky DC-bus capacitors to improve the system performance. In this case, the DC capacitance is designed for the second-order ripple frequency instead of the switching frequency, so it can not be reduced even when SiC MOSFETs are adopted to achieve high switching frequency. Although various topologies of three-phase four-wire inverters has been proposed to provide the path for neutral currents, they cannot handle the second-order ripples. Also, some active power decoupling solutions can be adopted, but they require additional active swithes and components, which increases the cost of the system. In this paper, a four-leg buck inverter is proposed, which consists of four DC-DC buck converters. Each buck converter is independently controlled. This topology can not only provide neutral currents, but also reduce the second-order ripples in the DC bus with active power decoupling control. The proposed topology doesn't require any additional active switches comparing to the conventional topologies with neutral legs. The effectiveness of proposed topology is verified by the simulation in MATLAB/Simulink.**

I. Introduction

Three-phase inverters have been widely used in the modern power system to integrate renewable energy resources into the grid, such as solar PVs and wind turbines. When the inverters are used to feed the unbalanced three-phase loads, the three-phase four-wire inverters are usually required to provide the current path for the zero-sequence currents, i.e. the neutral currents.

There are various topologies of three-phase four-wire inverters. The simplest one is the conventional three-phase three-leg inverter with the split DC bus capacitors [1][2][3], which connects the neutral point of the AC loads to the midpoint of the DC bus. This topology is called split-link topology. The split-link topology is the simplest and uses the least semiconductors (only six switches). However, the voltage balancing of the split capacitors is difficult [2] and the large capacitance is required to attenuate the voltage variation of the split capacitors.

Another topology is the three-phase four-leg inverter, which adds a fourth leg to the three-leg inverter for providing neutral currents [4][5][6]. This fourth leg is called the neutral leg. The four-leg inverter can be controlled by three-dimensional space vector modulation (3DSVPWM) [7], which has the advantage of 15% higher utilization of the DC-bus voltage comparing to the split-link topology. The main drawback of this topology is the electromagnetic interference (EMI) problems caused by the high-frequency operation of the neutral leg [8]. Also, the control of the neutral leg is coupled with the control of the three-phase inverter.

The third topology is the three-phase inverter with an independently-controlled neutral leg [9][10][11]. This topology is a combination of the aforementioned two topologies by connecting the midpoint of the split DC bus to the neutral leg. In this way, the neutral current can flow through the neutral leg and the neutral inductor instead of the split capacitors with active control. As a result, voltage balancing of the split capacitors can be maintained and the capacitance can be reduced. Moreover, this topology also allows the independent control of the neutral leg and avoids EMI problems of the four-leg inverter [12][13].

For three-phase four-wire inverters supplying unbalanced loads, besides the neutral currents, another challenge is the second-order ripples in the DC bus. The instantaneous output power on the AC side can be calculated as [14]:

$$p_{ac} = P_o + p_{2\omega} = P_o + P_{2\omega}\cos(2\omega t + \phi) \tag{1}$$

where P_o is the average value of the output power; $P_{2\omega}$ and ϕ are the amplitude and phase angle of the second-order power ripple $p_{2\omega}$ respectively. The second-order power ripple will inevitably propogate to the DC bus and cause second-order voltage and current ripples in the DC bus. Although the topologies mentioned above can provide neutral currents for unbalanced loads, they cannot handle the second-order ripples in the DC bus. It is often required to limit such ripples because they can deteriorate system performance [15]. Bulky DC-bus capacitors can be used to mitigate the ripples but will increase the weight and volumn of the system.

Normally, with the application of SiC MOSFETs, the converter can be operated at higher switching frequency with high efficiency so that the filter components and heat sinks can be

reduced to achieve high power density [16]. However, in the case of three-phase four-wire converters, since the bulky DC-bus capacitors are designed for the second-order frequency instead of the switching frequency, the power density of the converter is still low even when SiC MOSFETs are adopted.

Many active power decoupling solutions has been proposed for single-phase and three-phase converters to reduce the second-order ripples and capacitance in the DC bus. These solutions need extra active circuits to store the ripple energy so that the ripple energy flowing through the DC bus can be reduced or even completely eliminated [17]. However, the extra active switches and other components increase the cost of the system.

In this paper, a four-leg buck inverter is proposed for three-phase four-wire systems. It is extended from single-phase H-bridge inverter proposed in [18]. The proposed four-leg buck inverter consists of four DC-DC buck converters. Each buck converter can be independently controlled. The four-leg buck inverter can not only provide neutral currents like the conventional topologies, but also reduce the DC-bus ripples with active power decoupling control. The second-order ripple energy can be stored in the filter capacitor of each buck converter so that it will not flow through the DC bus. The proposed topology doesn't require any additional active switches comparing to the conventional topologies with neutral legs.

The rest of this paper is organized as follows. In Section II, the four-leg buck inverter is proposed and its operation principle is introduced. In Section III, the control strategy of the four-leg buck inverter is presented. In Section IV, the simulation results of different scenarios are presented to verify the proposed topology and control strategy. Finally, the conclusions are drawn in Section V.

II. Principle of the Four-leg Buck Inverter

As shown in Fig. 1 and Fig. 2, the proposed three-phase four-wire inverter consists of four DC-DC buck converters. Therefore, it is called the four-leg buck inverter. It consists of three phase legs and one neutral leg. The phase legs are connected to the three-phase loads or three-phase grid and the neutral leg is connected to the neutral point of the loads or the grid.

A. Without Active Power Decoupling Control

Firstly, the active power decoupling controller is not considered. Since the output voltage of a buck converter can never be negative, a DC offset voltage $\frac{1}{2}V_{dc}$ is added on the sinusoidal three-phase voltages as the voltage reference of the phase-leg buck converters:

$$\begin{cases} v_{Ca} = V_o \sin(\omega t) + \frac{1}{2}V_{dc} \\ v_{Cb} = V_o \sin\left(\omega t - \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} \\ v_{Cc} = V_o \sin\left(\omega t + \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} \end{cases} \tag{2}$$

The neutral-leg buck converter is controlled to generate only the DC offset voltage $\frac{1}{2}V_{dc}$:

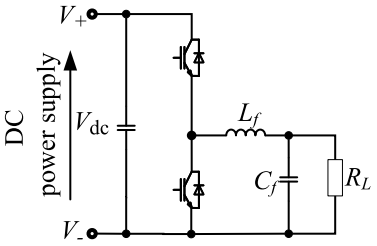


Figure 1. Buck converter.

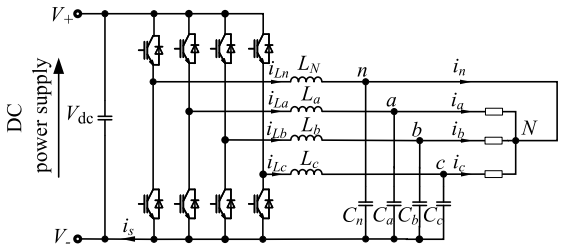


Figure 2. The proposed four-leg-buck inverter.

$$v_{Cn} = \frac{1}{2}V_{dc} \tag{3}$$

In this way, the symmetrical sinusoidal three-phase voltages can be obtained from the output of the four-leg buck inverter:

$$\begin{cases} v_{an} = v_{Ca} - v_{Cn} = V_o \sin(\omega t) \\ v_{bn} = v_{Cb} - v_{Cn} = V_o \sin\left(\omega t - \frac{2}{3}\pi\right) \\ v_{cn} = v_{Cc} - v_{Cn} = V_o \sin\left(\omega t + \frac{2}{3}\pi\right) \end{cases} \tag{4}$$

B. With active power decoupling control

The four-leg buck inverter is able to decouple the second-order ripples from the DC bus by actively control the output voltages of the buck converters. The second-order power ripple can then be stored in the filter capacitors C_a, C_b, C_c and C_n so that it will not flow through the DC bus. To realize the active power decoupling control, a second-order decoupling voltage v_{de} is applied to all the outputs of the buck converters:

$$\begin{cases} v_{Ca} = V_o \sin(\omega t) + \frac{1}{2}V_{dc} + v_{de} \\ v_{Cb} = V_o \sin\left(\omega t - \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} + v_{de} \\ v_{Cc} = V_o \sin\left(\omega t + \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} + v_{de} \\ v_{Cn} = \frac{1}{2}V_{dc} + v_{de} \end{cases} \tag{5}$$

$$v_{de} = V_{de} \sin(2\omega t + \theta_{de}) \tag{6}$$

As shown in (7), by adding the same decoupling voltages to all the buck converters, the phase voltages will not be affected:

$$\begin{cases} v_{an} = v_{Ca} - v_{Cn} = V_o \sin(\omega t) \\ v_{bn} = v_{Cb} - v_{Cn} = V_o \sin\left(\omega t - \frac{2}{3}\pi\right) \\ v_{cn} = v_{Cc} - v_{Cn} = V_o \sin\left(\omega t + \frac{2}{3}\pi\right) \end{cases} \tag{7}$$

The currents through the filter capacitors can be calculated as:

$$\begin{cases} p_{Ca} = v_{Ca} i_{Ca} = \frac{1}{2}\omega C_a V_o^2 \cos(2\omega t) + \left(\frac{1}{2}V_{dc} + v_{de}\right)\omega C_a V_o \cos(\omega t) + V_o \sin(\omega t)\, 2\omega C_a V_{de} \cos(2\omega t + \theta_{de}) \\ \qquad + \left(\frac{1}{2}V_{dc} + v_{de}\right) 2\omega C_a V_{de} \cos(2\omega t + \theta_{de}) \\ p_{Cb} = \frac{1}{2}\omega C_b V_o^2 \cos\left(2\omega t + \frac{2}{3}\pi\right) + \left(\frac{1}{2}V_{dc} + v_{de}\right)\omega C_b V_o \cos\left(\omega t - \frac{2}{3}\pi\right) + V_o \sin\left(\omega t - \frac{2}{3}\pi\right) 2\omega C_b V_{de} \cos(2\omega t + \theta_{de}) \\ \qquad + \left(\frac{1}{2}V_{dc} + v_{de}\right) 2\omega C_b V_{de} \cos(2\omega t + \theta_{de}) \\ p_{Cc} = \frac{1}{2}\omega C_c V_o^2 \cos\left(2\omega t - \frac{2}{3}\pi\right) + \left(\frac{1}{2}V_{dc} + v_{de}\right)\omega C_c V_o \cos\left(\omega t + \frac{2}{3}\pi\right) + V_o \sin\left(\omega t + \frac{2}{3}\pi\right) 2\omega C_c V_{de} \cos(2\omega t + \theta_{de}) \\ \qquad + \left(\frac{1}{2}V_{dc} + v_{de}\right) 2\omega C_c V_{de} \cos(2\omega t + \theta_{de}) \\ p_{Cn} = v_{Cn} i_{Cn} = \left(\frac{1}{2}V_{dc} + v_{de}\right) 2\omega C_n V_{de} \cos(2\omega t + \theta_{de}) \end{cases} \tag{9}$$

$$\begin{cases} i_{Ca} = C_a \frac{\mathrm{d}}{\mathrm{d}t} v_{Ca} = \omega C_a V_o \cos(\omega t) \\ \qquad +2\omega C_a V_{de} \cos(2\omega t + \theta_{de}) \\ i_{Cb} = C_b \frac{\mathrm{d}}{\mathrm{d}t} v_{Cb} = \omega C_b V_o \sin\left(\omega t - \frac{2}{3}\pi\right) \\ \qquad +2\omega C_b V_{de} \cos(2\omega t + \theta_{de}) \\ i_{Cc} = C_c \frac{\mathrm{d}}{\mathrm{d}t} v_{Cc} = \omega C_c V_o \sin\left(\omega t + \frac{2}{3}\pi\right) \\ \qquad +2\omega C_c V_{de} \cos(2\omega t + \theta_{de}) \\ i_{Cn} = C_n \frac{\mathrm{d}}{\mathrm{d}t} v_{Cn} = 2\omega C_n V_{de} \cos(2\omega t + \theta_{de}) \end{cases} \tag{8}$$

The instantaneous power of the filter capacitors can be calculated as shown in (9) according to (5) and (8):

Assuming $C_a = C_b = C_c = C_n$, the total instantaneous power of the filter capacitors can be obtained:

$$\begin{aligned} p_C &= p_{Ca} + p_{Cb} + p_{Cc} + p_{Cn} && (10) \\ &= 4\omega C_n V_{de} V_{dc} \cos(2\omega t + \theta_{de}) \\ &\quad + 2\omega C_n V_{de}^2 \cos(4\omega t + 2\theta_{de}) && (11) \\ &= p_{C\_2\omega} + p_{C\_4\omega} \end{aligned}$$

where

$$p_{C\_2\omega} = 4\omega C_n V_{de} V_{dc} \cos(2\omega t + \theta_{de}) \tag{12}$$

$$p_{C\_4\omega} = 2\omega C_n V_{de}^2 \cos(4\omega t + 2\theta_{de}) \tag{13}$$

According to (1) and (10), the second-order power ripple from the unbalanced loads can be compensated by the filter capacitors if the following equation can be satisfied:

$$p_{2\omega} = p_{C\_2\omega} \tag{14}$$

Therefore, the amplitude and phase angle of v_{de} can be then calculated:

$$\begin{cases} V_{de} = \frac{P_{2\omega}}{4\omega C_n V_{dc}} \\ \theta_{de} = \phi \end{cases} \tag{15}$$

where $P_{2\omega}$ and ϕ are the amplitude and phase angle of the second-order power ripple $p_{2\omega}$ respectively as shown in (1). In this way, the second-order power ripple can be stored in the filter capacitors so that it will not flow through the DC bus. According to (13), although the second-order power ripple on the DC bus is compensated, another 4^{th}-order power ripple $p_{C\_4\omega}$ is introduced by the v_{de} and it will cause 4^{th}-order ripples on the DC bus. However, the amplitude of $p_{C\_4\omega}$ is much smaller than $P_{2\omega}$ because V_{de} should be less than 10% to reduce the DC-bus voltage requirement. Therefore, the 4^{th}-order power ripple introduced by v_{de} is less than 5% of the second-order ripples:

$$\frac{|p_{C\_4\omega}|}{|p_{C\_2\omega}|} = \frac{V_{de}}{2V_{dc}} \leq 5\% \tag{16}$$

The total ripples in the DC bus are reduced.

III. Control Strategy

The control strategy of the proposed four-leg buck inverter is shown in Fig. 3. Each buck converter is independently controlled by the inner current-loop controller $G_{PR\_i}(s)$ and the outer voltage-loop controller $G_{PR\_v}(s)$. The output voltages of the four-leg buck inverter are balanced three-phase sinusoidal voltages. Both $G_{PR\_i}(s)$ and $G_{PR\_v}(s)$ are proportional-resonant controllers with the resonant peak at the fundamental frequency:

$$G_{PR\_v}(s) = K_{p\_v} + \frac{2\xi_v \omega s}{s^2 + 2\xi_v \omega s + \omega^2} \times K_{R\_v} \tag{17}$$

$$G_{PR\_i}(s) = K_{p\_i} + \frac{2\xi_i \omega s}{s^2 + 2\xi_i \omega s + \omega^2} \times K_{R\_i} \tag{18}$$

where K_{p_v} and K_{p_i} are the proportional gains of the voltage and current contrller respectively; K_{R_v} and K_{R_i} are the resonant gains of the voltage and current controllers respectively; ξ_v and ξ_i are the coefficients of cut-off frequency.

As shown in Fig. 3, the reference signals for the phase-leg controllers are the balanced sinusoidal three-phase voltages and the feedback signals are the phase-to-ground voltages of the three-phase loads. The reference signal for the neutral leg controller is $\frac{1}{2}V_{dc}$ and the feedback signal is the voltage of the capacitor C_n.

In the active power decoupling controller, the DC-bus current i_s is measured as the feedback and controlled by the resonant controller $G_{R\_de}(s)$ to generate the decoupling voltage v_{de}:

$$G_{R\_de}(s) = \frac{2\xi_{de}(2\omega)\, s}{s^2 + 2\xi_{de}(2\omega)\, s + (2\omega)^2} \times K_{R\_de} \tag{19}$$

where ξ_{de} defines the cut-off frequency; K_{R_de} is the resonant gain of the controller. The gain of $G_{R\_de}(s)$ is almost zero everywhere apart from the resonant frequency 2ω. Therefore, the DC component of the DC-bus current has no effect to the output of the resonant controller. v_{de} is then added to the

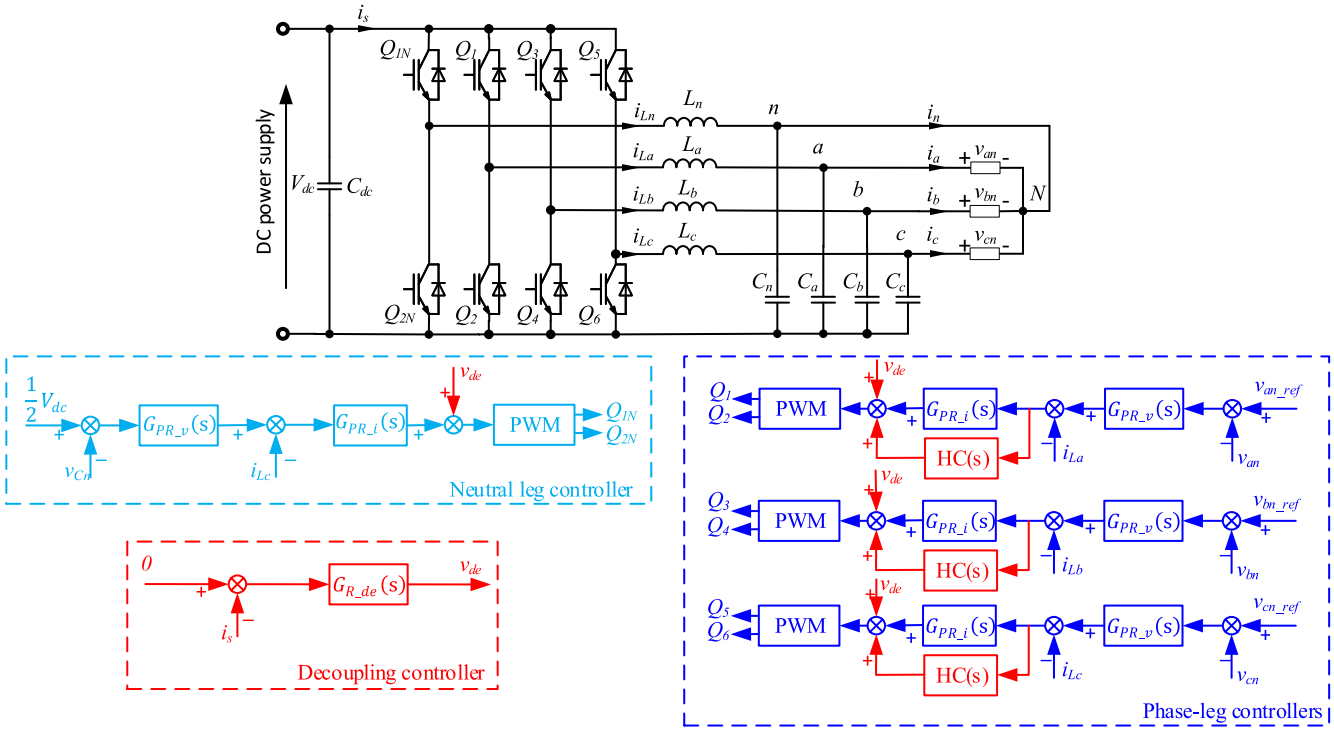


Figure 3. Control strategy of the four-leg-buck inverter.

voltage references generated by the current-loop controllers of the phase legs and the neutral leg.

According to (7), there is no second-order harmonics introduced to the load voltages theoretically. However, in the practical implementation, the second-order harmonics will still be introduced to the loads by v_{de} due to the mismatch of the filter inductors and capacitors. Therefore, the harmonic compensators (HC) are added in the current loops of the phase-leg controllers to compensate the second-order harmonics in the loads:

$$HC\left(s\right)=\frac{2\xi_{HC}\left(2\omega\right)s}{s^{2}+2\xi_{HC}\left(2\omega\right)s+\left(2\omega\right)^{2}}\times K_{HC}. \tag{20}$$

where ξ_{HC} defines the cut-off frequency of $HC\left(s\right)$; K_{HC} is the resonant gain of the controller. The resonant frequency of $HC\left(s\right)$ is 2ω to compensate the second-order harmonics.

IV. Simulation Results

The proposed four-leg buck inverter and the proposed control strategy are verified by simulation in MATLAB/Simulink. The simulation parameters are shown in Table I. The switching frequency is set as 20 kHz. Since each leg of the inverter is a buck converter, the DC bus voltage should be higher than the peak value of the voltage of the filter capacitor. The DC-bus voltage is set as 720 V in the simulation.

Three different scenarios are simulated:

- Scenario I - Balanced loads: $R_a = R_b = R_c = 50\,\Omega$.
- Scenario II - Unbalanced loads without active power decoupling controller: $R_a = R_b = 50\,\Omega$, $R_c = 100\,\Omega$.

Table I
Simulation Parameters.

DC voltage	720 V
AC output voltage	230 Vrms
Filter inductors	2.5 mH
Filter capacitors	20 μF
Switching frequency	20 kHz

- Scenario III - Unbalanced loads with active power decoupling controller: $R_a = R_b = 50\,\Omega$, $R_c = 100\,\Omega$.

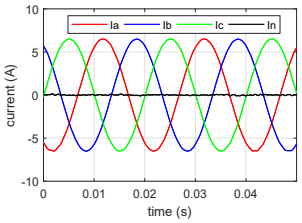
A. Scenario I and II

The simulation results of Scenario I and II are shown in Fig. 4 and Fig. 5. It can be seen that the proposed four-leg buck inverter can feed both balanced and unbalanced three-phase loads with balanced sinusoidal voltages.

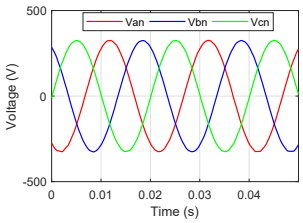
Under the balanced load condition, the three-phase currents are balanced and the neutral current is nearly zero. Besides, there is no second-order current ripples in the DC bus since there is no second-order power ripple under the balanced load condition.

Under the unbalanced load condition, the three-phase currents are unblanced and the neutral current is provided by the neutral leg buck converter. The DC-bus current I_{dc} contains second-order current ripples due to the unbalanced loads.

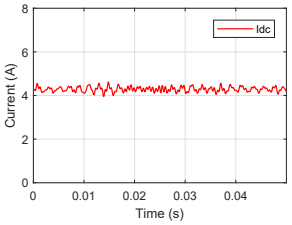
In both Scenario I and II, The capacitor voltages are shown in Fig. 4d and 5d respectively. It can be seen that the capacitor volatges of the phase legs are sinusoidal voltages with DC offset $\frac{1}{2}V_{dc}$ according to (2). And the capacitor voltages of the neutral leg is $\frac{1}{2}V_{dc}$ according to (3). The simulation results of



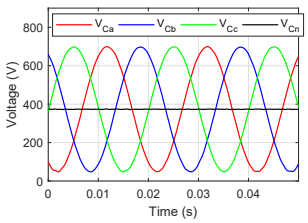
(a) Load currents.



(b) Load voltages.

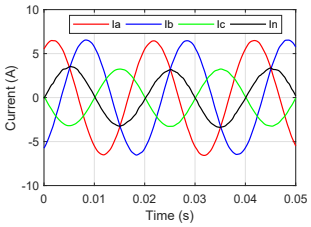


(c) DC-bus current I_{dc}.

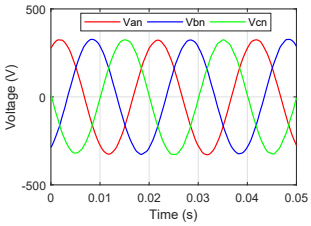


(d) Capacitor voltages.

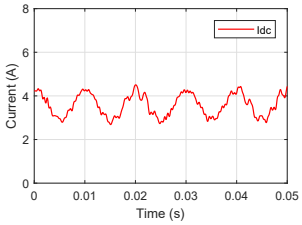
Figure 4. Simulation results with balanced loads (Scenario I).



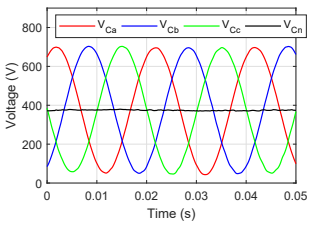
(a) Load currents.



(b) Load voltages.



(c) DC-bus current I_{dc}.



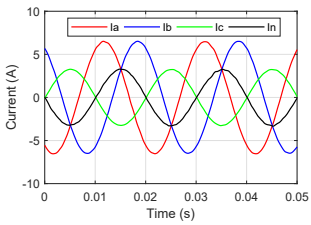
(d) Capacitor voltages.

Figure 5. Simulation results with unbalanced loads without active power decoupling control (Scenario II).

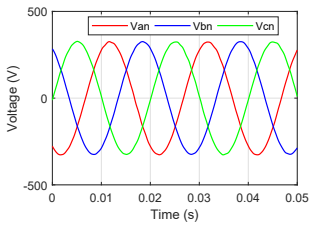
Scenario I and II prove that the proposed four-leg buck inverter can feed the three-phase loads, either balanced or unbalanced loads, which is the basic function of three-phase four-wire inverters.

B. Scenario III

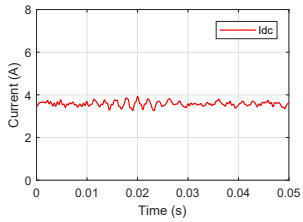
The simulation results of Scenario III are shown in Fig. 6. In Scenario III, the active power decoupling controller is added to reduce the second-order ripples in the DC bus under unbalanced conditions. Comparing to the simulation results of Scenario II, the load currents and voltages in Scenario III are the same because the loads are not changed. However, in Scenario III, as shown in Fig. 6c, the second-order current



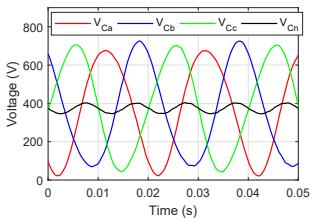
(a) Load currents.



(b) Load voltages.



(c) DC-bus current I_{dc}.



(d) Capacitor voltages.

Figure 6. Simulation results with unbalanced loads with active power decoupling control(Scenario III).

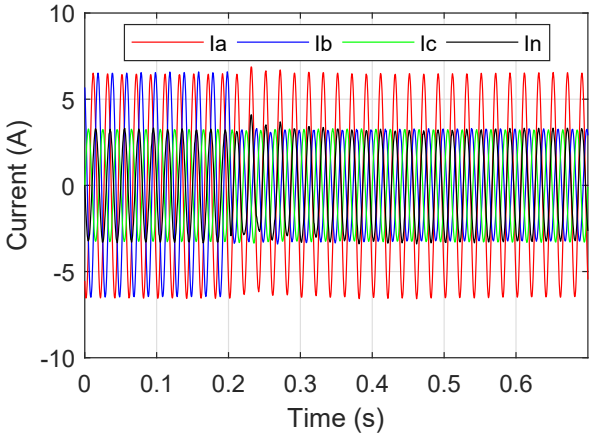
ripples in the DC bus are significantly reduced comparing to the simulation result of Scenario II in Fig. 5c. In Fig. 6d, the capacitor voltages contain second-order voltages according to (5) due to the decoupling controller. It has been illustrated in Section II that these second-order voltages will not affect the output phase voltages of the inverter according to (7), as shown in Fig. 6b.

C. Transient response

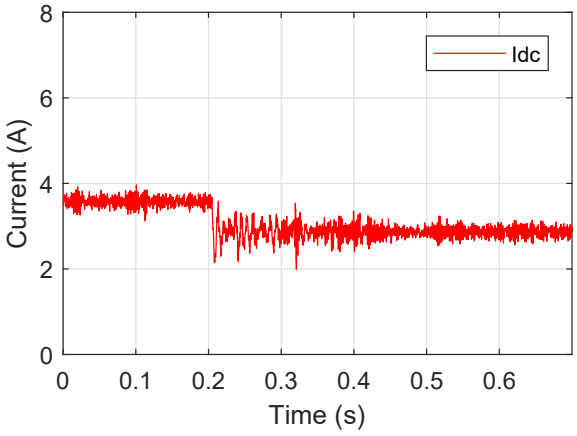
The transient response of a step load change in phase b is simulated. Before the step load change, the load condition is $R_a = R_b = 50\,\Omega$, $R_c = 100\,\Omega$. At 0.2 s, R_b is changed from $50\,\Omega$ to $100\,\Omega$. The simulation results of load currents and DC-buc current are presented in Fig. 7. As shown in Fig. 7b, the transient response of the DC-bus current takes around 0.2 s (10 fundamental cycles).

V. Conclusions

In this paper, a four-leg buck inverter is proposed, which is a three-phase four-wire inverter consists of four DC-DC buck converters. Each buck converter can be independently controlled. The principle and control strategy of the four-leg buck inverter is presented. The proposed inverter can feed the three-phase unbalanced loads and provide neutral currents like the conventional three-phase four-wire inverters. Also, it can reduce the second-order ripples in the DC bus with the active power decoupling controller. Simulation results are presented to verify the effectiveness of the proposed topology in different scenarios. It should be mentioned that the proposed inverter doesn't require any additional active switches comparing to the conventional topologies with neutral legs. The future work is to build the four-leg buck inverter with SiC MOSFETs to test the perfermance including the efficiency analysis.



(a) Load currents.



(b) DC-bus current I_{dc}.

Figure 7. Simulation results of transient response (step load change in phase b).

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