# DC Current Flow Controller with Fault Current Limiting and Interrupting Capabilities

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***Abstract*- Conventionally, the current flow control and DC fault protection issues of HVDC grids are supposed to be solved by the DC current flow controller (CFC) and DC circuit breaker (DCCB) separately, which may result in a high capital cost. This paper proposes a CFC topology with DC fault current limiting and interrupting capabilities. The topology and operating principle of the CFC are presented with theoretical analysis. The control strategies under normal and fault conditions are described. In order to reduce the use of IGBTs, an H-bridge inter-line CFC with fault current limiting capability is further proposed based on the proposed CFC. The proposed CFCs are tested in PSCAD/EMTDC. Simulation results show that the proposed two CFCs can effectively control the current flow of two lines during normal operation and limit and interrupt DC fault currents.**

**Index Terms—HVDC grids, Current flow controls, Fault current limiting, DC Current Breaker.**

## I. Introduction[1]

THANKS to its fast development, the high-voltage direct-current (HVDC) grid technology has been recognized as an effective solution for renewable energy grid connection and consumption [1]-[3]. The HVDC grid is the next logical step of the HVDC network which does not have the redundant operation capability. In an HVDC grid, there are multiple (at least two) transmission lines connecting to each converter, which improves the flexibility and reliability of the overall system. However, it may complicate its current flow control and fault protection. An HVDC grid may lack control freedom for managing its internal current flow if the number of DC lines is greater than the number of converters. In this case, a DC current flow controller (CFC) may be an effective solution.

Different types of CFCs have been proposed in the open literature [4]-[13]: variable resistors, DC/DC converter, auxiliary voltage sources and inter-line CFC. Variable resistors can change DC line currents by adjusting their equivalent resistance. However, they will consume power during its operation [4]. The DC/DC converter deployed within a DC line can regulate its terminal voltage to control the DC current flow [4]-[8]. However, it involves a number of power electronics devices and therefore, result in a high cost. The auxiliary voltage source absorbs power from the AC side and injects it to the DC side. However, they are designed to connect to the converter valve-side wherein a high requirement of the insulation and cost are needed [9].

The inter-line CFC controls the current flow by exchanging the power between two lines. There are two types of inter-line CFCs. One is to connect capacitors in series to two different lines at different times, which is equivalent to connecting a voltage source in series in the line. The structure is simple and has a low cost. However, it may lead to DC current ripples [10]. The other connects two capacitors into two lines, and the capacitors are connected by a bidirectional flow DC/DC converter. Controlling the power exchange between the capacitors can regulate the current flow of the two lines [11]-[13].

Apart from the DC current flow management, the DC fault protection of HVDC grids is one of the main bottlenecks of their wide applications. The DC circuit breaker (DCCB) can be an enabler. The parallel mechanical DCCB proposed in [14] can interrupt a 15 kA DC current within 5 ms. ABB developed a hybrid DCCB which solves the issues of on-state power losses and operating speed [15]. However, the capability of current interruption is limited considering the capital cost and system complexity. To reduce the burden of current interrupting devices in DCCBs, fault current limiters (FCLs) can be employed [16]-[21].

A hybrid FCL consists of a current-limiting inductor (CLI) and a parallel energy dissipation circuit (EDC) has been proposed in [18]. The EDC consists of thyristor-controlled resistors, and is able to accelerate the current interruption. The hybrid FCL proposed in [19] contains thyristors, capacitors and inductors. An effective method for fast bypassing the FCL inductor was proposed to reduce the energy dissipation when DCCB acts. But the capacitors need to be pre-charged to a certain value to control the thyristors. The FCLs proposed in [20] and [21] have functions both of the DCCB and FCL. The former needs many branches, and the latter is mainly applicable to DC microgrids.

To reduce the use of additional switches and devices, studies have been conducted to combine a CFC with a fault current limiter and interrupter. The series-parallel multifunctional

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composite controller in [22] can realize current flow control and fault current limiting. However, this topology is mainly used in power distribution networks because it uses the DC/DC structure and therefore, the inverter side needs to withstand DC line-level high voltage. Reference [23] proposes a current flow controlling circuit breaker (CB), which combines the inter-line CFC in [10] with fault current breaking capability. In [24], the load commutating switch (LCS) used in the hybrid DCCB is built in the inter-line CFC. However, the CFCs in [23] and [24] do not have fault current limiting capabilities.

To bridge the abovementioned research gaps, this paper proposes a CFC with fault current limiting and interrupting capabilities. In this CFC, the inductor and capacitors are utilized in two conditions. In normal condition, the inductor exchange power with capacitors to control current flows of two lines. The inductor will be kept in the DC line to limit the current when a pole-to-ground fault occurs on either transmission line. The voltage of the capacitor is used to control the thyristors to interrupt the fault current. Moreover, the inductor is automatically bypassed when the fault current reaches its peak, which helps to accelerate the decay of the fault current. The effectiveness of the proposed CFC has been verified through simulations performed in PSCAD/EMTDC, with simulation results and the theoretical analysis showing a good agreement.

## II. Topology and Operational Mechanism of the Proposed CFC

### A. Topology of the Proposed CFC

As shown in Fig. 1, the proposed CFC consists of a CFC with a current limiting capability and two CBs. Fig. 1(a) shows the topology of the proposed CFC and Fig. 1(b) shows the configuration of the two CBs. The CFC consists of two controllable capacitors ($C_1$, $C_2$) connected in two lines, an inductor ($L$), eight IGBTs ($V_1$ ~ $V_8$) and their series connected diodes, and four groups of series connected IGBTs ($V_{11}$ ~ $V_{14}$) and their anti-paralleled diodes.

Taking CB1 as an example. It has two capacitors ($C_{10}$, $C_{20}$), two bidirectional switches ($S_1$, $S_2$), two sets of auxiliary switches ($V_{1a}$, $V_{1b}$) and their anti-paralleled diodes, two ultra-fast disconnectors ($UFD_1$, $UFD_2$), four sets of anti-paralleled thyristors ($T_{1a}$, $T_{1b}$),…, ($T_{4a}$, $T_{4b}$) and two arresters.

During normal operation, $UFD_1$ and $UFD_2$ are closed, $V_{1a}$ and $V_{1b}$ are closed, ($T_{1a}$, $T_{1b}$),…, ($T_{4a}$, $T_{4b}$) are turned off, ($S_1$, $S_2$) and ($V_{1a}$, $V_{1b}$) are turned on. In this case, the two CBs are locked. The proposed circuit operates as a CFC. The CFC function will be immediately locked if a pole-to-ground fault is detected. Based on the discrimination of the faulted line and its current direction, the inductor $L$ will be switched into the faulted line to limit the fault current by controlling $V_{11}$~$V_{14}$ and $V_1$~$V_8$.

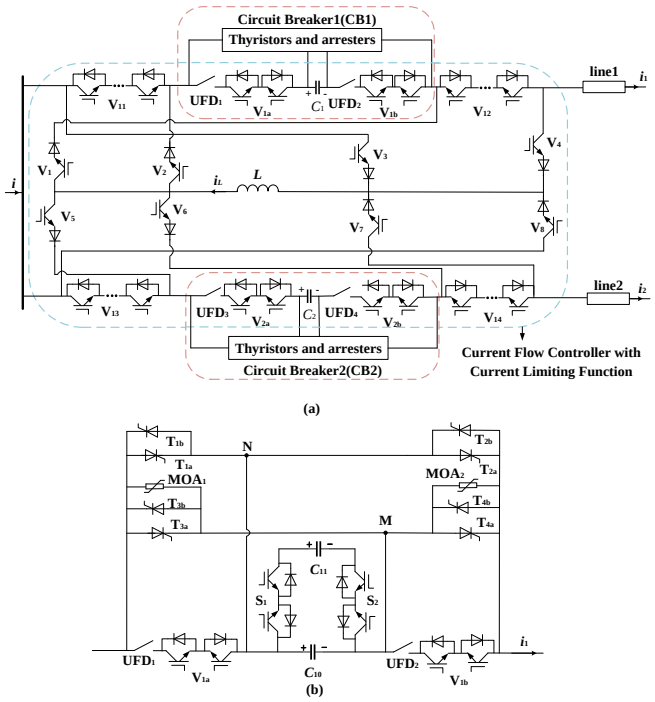


Fig. 1. Topology of the proposed CFC. (a) Overall structure diagram; (b) Structure of CB1.

### B. Operating Principle of the Proposed CFC

#### a. DC current flow control

The energy exchange between the inductor $L$ and equivalent capacitors $C_1$ and $C_2$ is achieved by controlling $V_1$~$V_8$ and therefore, resulting in the regulation of the current flows of lines 1 and 2. The positive direction of each current is shown in Fig.1. In the following analysis, when the current direction is negative, an increase of the current's absolute value indicates a current increase. Moreover, it is assumed that the input current $i$ is constant during the current flow controlling process. If $i_1$ and $i_2$ are in the same direction, the increase of one current will lead to a decrease of the other, and vice versa. The operation will be described below if the directions of $i_1$ and $i_2$ are different.

Taking $i_1$ is positive and $i_2$ is negative and $i_1$ is being increased as an example. First, turning on $V_1$ and $V_3$ to make $C_1$ and $L$ parallel connected. In this case, $C_1$ will charge $L$ and the current in $L$ will gradually increase. The current direction of $L$ is positive, as shown in Fig. 2(a). After a short period of time, $C_2$ will be connected in parallel with $L$ when $V_1$ and $V_3$ are turned off and $V_5$ and $V_7$ are turned on. In this case, $L$ will charge $C_2$ and the current in $L$ will gradually decrease and the current direction is still positive, as shown in Fig. 2(b). The above process is performed once in one switching cycle and will be repeated at a high switching frequency in normal operation. In steady state, the voltages of the two equivalent capacitors remain constant. It is equivalent to deploying a voltage source in each line whose equivalent circuit is shown in Fig. 3.

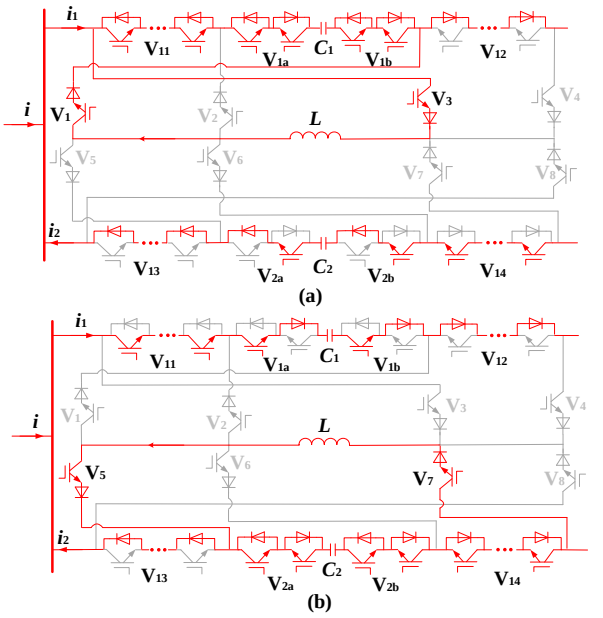


Fig. 2. Operation principle in case of reversed current directions. (a) $L$ and $C_1$ in parallel; (b) $L$ and $C_2$ in parallel.

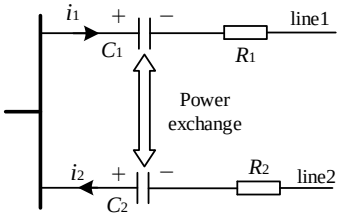


Fig.3. Equivalent circuit of the current flow control.

*b. Fault current limiting*

Assuming $i_1$ is positive and $i_2$ is negative and a pole-to-ground fault occurs on line 1. Blocking signals will be sent to $V_1$, $V_3$, $V_5$, and $V_7$ to lock the current flow control function when the fault is detected. After a period of equipment delay, $V_{11}$ will be turned off and $V_2$ and $V_3$ will be turned on. The inductor $L$ will then be switched in the faulted line 1 to limit the fault current. Current directions during the rising of the fault current are shown as the solid lines in Fig. 4. The fault current starts to decrease when it reaches the maximum value. In this case, the voltage of $L$ is shown in Fig. 4. The fault current flows through the anti-parallel diode on $V_{11}$, as indicated by the dashed line, the inductor $L$ is bypassed.

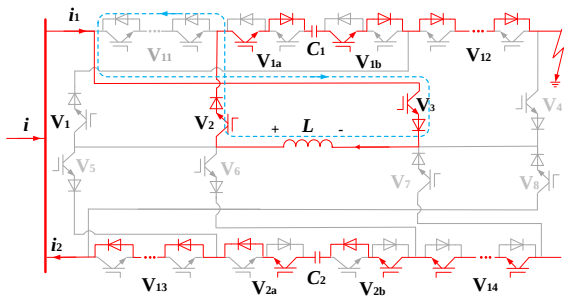


Fig. 4. Operation of the fault current limiting.

Each converter station may feed current to the fault point, and the current on each line will increase. As shown in Fig. 4, $C_2$ will be charged by the current $i_2$. In this way, $C_2$ helps to reduce the current feeds to line 1 .

*c. Fault current clearance*

Assuming the output current of the converter station is positive and the fault occurs on line 1. There are two different conditions:

Condition 1: The initial direction of $i_1$ is positive and the current will remain positive after the fault. Condition 2: The initial direction of $i_1$ is negative, after the fault, the current will firstly decrease to zero and then start to increases in the opposite direction.

In both conditions, there are two status of the voltage $u_{C1}$ on $C_1$: positive and negative. For condition 1, taking $u_{C1}$ is positive as an example, the operating processes are as follows:

1) In normal operation, the CFC controls current flows according to system requirements. $UFD_1$ and $UFD_2$ are closed, $V_{1a}$ and $V_{1b}$ are turned on, as shown in Fig. 5 (a).

2) $V_{1a}$ and $V_{1b}$ will be turned off, $T_{1a}$ and $T_{2a}$ will be triggered after detecting the fault. The current will be transferred to branch $T_{1a}$ and $T_{2a}$. The current flows through $C_1$ is zero. $S_1$, $S_2$ and $UFD_1$, $UFD_2$ are turned off, as shown in Fig. 5 (b).

3) Once $UFD_1$ and $UFD_2$ are fully opened, $T_{3a}$ will be triggered and it will be turned on due to the positive voltage. $C_{10}$ begins to discharge, and the current will shifts from the $T_{1a}$ branch to the $T_{3a}$ branch.

4) When the voltage of $C_{10}$ drops to zero, it will continue to be reverse-charged, and the capacitor voltage will increase continuously as shown in Fig. 5(c). $MOA_2$ will be turned on when the capacitor voltage reaches MOA's critical voltage, as shown in Fig. 5(d). The fault current energy will be dissipated by the arrester.

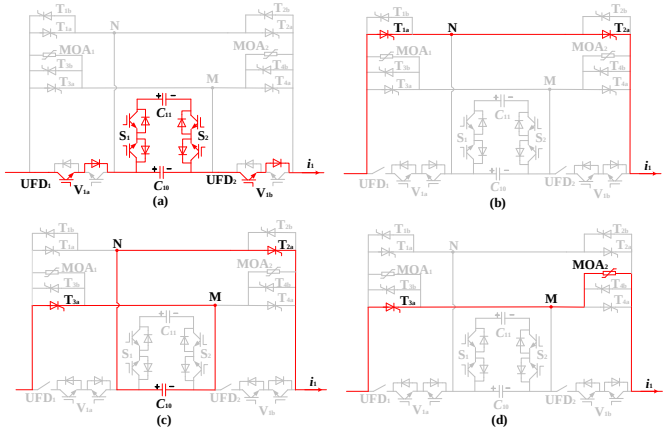


Fig. 5. Operation principle of the fault current clearance. (a) Stage I; (b) Stage II; (c) Stage III; (d) Stage IV.

If $u_{C1}$ is negative in step 3), $T_{4a}$ will be triggered instead of $T_{3a}$ and therefore, in step 4), $MOA_1$ will be turned on. For condition 2, if $u_{C1}$ is positive, $T_{1a}$, $T_{2a}$, $T_{1b}$ and $T_{2b}$ will be turned on to ensure fault current flows once the fault is

detected in step 2). Then, the following processes will be the same as condition 1. The control diagram and the control sequences of the proposed CFC are illustrated in Fig. 6.

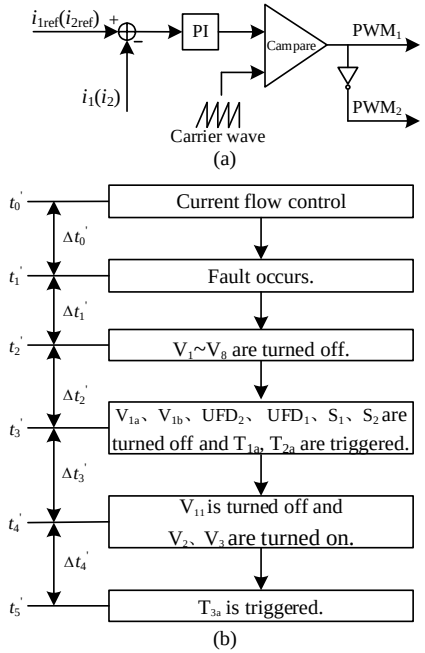


Fig.6. Control of the proposed CFC. (a) Control diagram; (b) Control sequences.

## III. Theoretical Analysis of the Operation Process

### *A. Theoretical Analysis of Current Flow Control*

First, assuming $i_1$ is positive and $i_2$ is negative and increasing $i_1$ to analyze the current flow control. Based on Fig. 1, $i_1$ can be calculated as follows:

$$i_1 = i \ + |i_2| . \tag{1}$$

Assuming that the output current $i$ of the converter station is constant. $i_1$ will increase if | $i_2$ | increases. Thus, the polarity of the voltage of $C_2$ is positive. If $V_1$ ~ $V_8$ are turned off, $C_2$ will continue to discharge to line 2. In order to maintain the stability of the capacitor energy, it is necessary to control the switches to perform energy transfer. If $i_1$ is positive and $i_2$ is negative, the switches need to be controlled are $V_1$, $V_3$, $V_5$, and $V_7$. $V_1$ and $V_3$ have a duty cycle of $D$, The switching of $V_5$ and $V_7$ are complementary. Assuming that the inductor current is continuous, it can be deduced from the volt-second characteristic:

$$\frac{u_{C_1}}{u_{C_2}} = \frac{1-D}{D} . \tag{2}$$

where $u_{C1}$ and $u_{C2}$ are the voltages of the capacitors $C_1$ and $C_2$ in the steady state. Then, the current flow of a DC gird with the proposed CFC can be analyzed as follows. Taking the four-terminal DC power grid shown in Fig. 7 as an example. Stations 1, 3 and 4 operate at constant power control modes. Station 2 controls the DC voltage. The proposed CFC is installed in the DC bus of station 1.

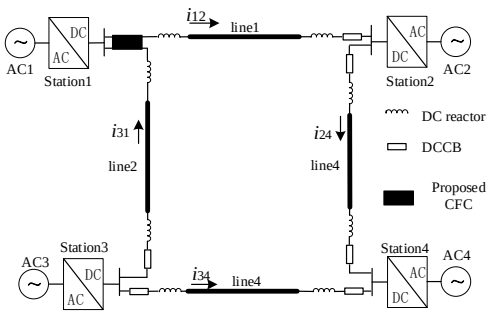


Fig. 7. Diagram of the four-terminal DC transmission system.

The current flow can be calculated by (3), where $u_1$, $u_2$, $u_3$, $u_4$ are the DC terminal voltages of the four converters, $P_1$, $P_3$, and $P_4$ are the power output from converters 1, 3, and 4 to the DC-side, $R_{12}$, $R_{13}$, $R_{34}$ and $R_{24}$ are the resistances of lines 1,2,3,4; $i_{12}$, $i_{13}$, $i_{34}$ and $i_{24}$ are the currents of lines 1,2,3,4.

$$\begin{cases} i_{12} = \left(u_1 - u_2 - u_{C_1}\right) / R_{12} \\ i_{13} = \left(u_1 - u_3 - u_{C_2}\right) / R_{13} \\ i_{24} = \left(u_2 - u_4\right) / R_{24} \\ i_{34} = \left(u_3 - u_4\right) / R_{34} \\ u_{C_1} i_{12} = -u_{C_2} i_{13} \end{cases} . \tag{3}$$

$$\begin{cases} P_1 = u_1\left(i_{12} + i_{13}\right) \\ P_3 = u_3\left(i_{34} - i_{13}\right) \\ P_4 = u_4\left(-i_{24} - i_{34}\right) \end{cases} . \tag{4}$$

It can be known from equations (2) and (3)

$$\left|\frac{i_{12}}{i_{13}}\right| = \frac{D}{1-D} . \tag{5}$$

### *B. Analysis of Fault Current Limiting and Clearance*

In the four-terminal DC power grid, the analysis and calculation of fault currents will be very complicated. Therefore, a simplified model with one equivalent converter is used to analyze the fault current limiting and interrupting of the proposed CFC. The equivalent circuit is shown as Fig. 8.

In Fig. 8, $u_{dc}$ is the equivalent DC voltage source of the converter station, $R_S$ is the equivalent resistor of the converter station, $L_{dc}$ is the DC reactor, and $R_l$ and $L_l$ are the equivalent resistor and inductor of the line. In this circuit, the current flow control cannot be performed. Before the fault occurs, the capacitor $C_{10}$ is pre-charged to $u_0$ to emulate the steady state operation. Before the fault occurs, $V_{11}$ and $V_{1b}$ are turned on, $UFD_1$ is closed, $V_2$, $V_3$ and thyristors are turned off.

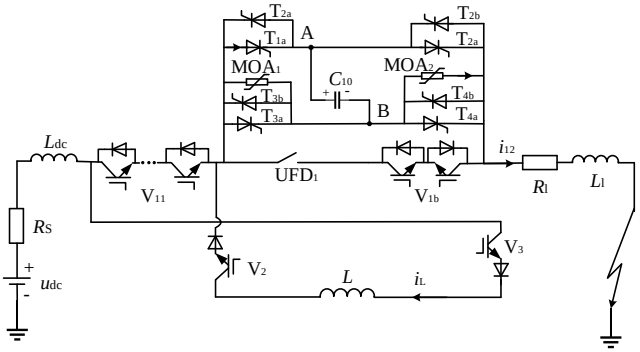


Fig. 8. Diagram of a test circuit.

TABLE I
SEQUENCES OF THE CURRENT LIMITING AND CLEARANCE PROCESSES

| Time | Current limiting and clearance processes |
|---|---|
| $t_0$ | Fault occurs. |
| $t_1$ | The fault is detected. |
| $t_2$ | $V_{1b}$, $UFD_1$ are turned off and $T_{1a}$, $T_{2a}$ are triggered. |
| $t_3$ | Current-limiting inductor is put in. |
| $t_4$ | $T_{3a}$ is triggered |
| $t_5$ | The fault current is at its peak |
| $t_6$ | Arrester acts |

1) $t_0$~$t_3$

The current starts to rise when the fault occurs at $t_0$. The pre-fault value of the current is $I_0$. At $t_2$, the devices start to operate. The on-state voltage drops of $V_{11}$ and $V_{1b}$ are ignored. During the period of $t_0$~$t_2$, the fault current $i_{12}$ is expressed as:

$$i_{12} = I_0 + \left( \frac{u_{dc}}{R_s + R_l} - I_0 \right) \left( 1 - e^{-\frac{(t-t_0)}{\tau_0}} \right), \tag{6}$$

where $\tau_0$ is defined as:

$$\tau_0 = \frac{L_{dc} + L_l}{R_s + R_l}.$$

Starting from $t_2$, and the current is transferred from the branch of $V_{1b}$, $UFD_1$ and $UFD_2$ to the branch of $T_{1a}$ and $T_{2a}$. During the period of $t_2$~$t_3$, regardless of the thyristor on-state power losses, the current is still expressed as equation (6).

2) $t_3$~$t_4$

At $t_3$, the current-limiting inductor $L$ is connected to the line, and the instantaneous magnetic flux is expressed as:

$$\begin{cases} \Psi(t_{3-}) = (L_{dc} + L_l) \cdot i_{12}(t_{3-}) \\ \Psi(t_{3+}) = (L_{dc} + L_l + L) \cdot i_{12}(t_{3+}) \end{cases} \tag{7}$$

It can be obtained from equation(7) that

$$i_{12}(t_{3+}) = \frac{L_{dc} + L_l}{L_{dc} + L_l + L} i_{12}(t_{3-}) \tag{8}$$

The current $i_{12}$ will suddenly change when $L$ is inserted into the circuit. After $t_{3+}$, $L$ is fully inserted into the line. It can be obtained from KVL that

$$u_{dc} = (L_{dc} + L_l + L) \frac{di_{12}}{dt} + (R_s + R_l) i_{12}. \tag{9}$$

The value of $i_{12}(t_{3+})$ can be obtained from (6) and (8). Substituting it into (9), the line fault current $i_{12}$ is expressed as

$$i_{12} = i_{12}(t_{3+}) + \left[ I_1 - i_{12}(t_{3+}) \right] \left( 1 - e^{-\frac{(t-t_3)}{\tau_1}} \right), \tag{10}$$

where all the variables are defined as:

$$\begin{cases} \tau_1 = \dfrac{L_{dc} + L_l + L}{R_s + R_l} \\ I_1 = \dfrac{u_{dc}}{R_s + R_l} \end{cases}.$$

3) $t_4$~$t_6$

At $t_4$, $T_{3a}$ is triggered. After $T_{3a}$ is turned on, the voltage of $C_1$ is imposed on both ends of $T_{1a}$ making it withstand the reversed voltage. The anode current drops rapidly, and $C_1$ starts to discharge. Due to the negative voltage provided by $C_1$, $T_{1a}$ will be automatically turned off when the current in it becomes zero. Then $C_1$ will be reversely charged until the arrester is triggered at $t_6$. Ignoring the on-state voltage drop of the thyristor during the period of $t_4$~$t_5$, it can be obtained from KVL and KCL that

$$\begin{cases} u_{C10} = \sqrt{d_1^2 + d_2^2} e^{\partial(t-t_4)} \sin\left( \omega(t - t_4) + \theta_1 \right) - u_{dc} \\ i_{12} = C_{10} \sqrt{(\partial^2 + \omega^2)(d_1^2 + d_2^2)} e^{\partial(t-t_4)} \sin\left( \omega(t - t_4) + \theta_2 \right) \end{cases}, \tag{11}$$

where all the variables are defined as:

$$\begin{cases} \partial = -\dfrac{R_s + R_l}{2(L_{dc} + L_l + L)} \\ \omega = \sqrt{\dfrac{1}{(L_{dc} + L_l + L) C_{10}} - \dfrac{(R_s + R_l)^2}{4(L_{dc} + L_l + L)^2}} \\ d_1 = u_0 + u_{dc}, d_2 = -\dfrac{i_{12}(t_4) + \partial d_1 C_{10}}{\omega C_{10}} \\ \tan\theta_1 = \dfrac{d_1}{d_2}, \tan\theta_1 = \dfrac{\partial d_1 + \omega d_2}{\partial d_2 - \omega d_1} \end{cases}$$

At $t_5$, the fault current reaches its maximum, and then the inductor $L$ is bypassed. During the period of $t_5$~$t_6$, the inductance in the circuit is changed from $L_{dc} + L_1 + L$ to $L_{dc} + L_1$. The capacitor voltage and fault current can be obtained by taking the new inductance into equation (11).

4) $t_6$<$t$

At $t_6$, the arrester operates with a clearance time of $\Delta t$. The energy dissipation process of the arrester is simplified. The voltage across the arrester is approximately expressed as $ku_{movn}$, where $u_{movn}$ is the rated voltage of the arrester and $k$ is a constant calculated

based I-V characteristic of the surge arrester to emulate arrester's voltage. During $\Delta t$, the following voltage relationship can be obtained based on KVL:

$$(L_{dc}+L_1)\frac{di_{12}}{dt}=-ku_{movn}+u_{dc}, \tag{12}$$

The value of $i_{12}(t_6)$ can be obtained from (11). Substituting (11) into (12), $i_{12}$ can be obtained as follows.

$$i_{12}=i_{12}(t_6)-\frac{ku_{movn}-u_{dc}}{L_{dc}+L_1}t. \tag{13}$$

*C. The Selection of Parameters*

Taking the capacitors $C_{10}$ and $C_{11}$ in line 1 as an example. It can be seen from (11) that, during the fault current clearance process, a large capacitance will result in a slow charging speed and large fault current. During the current flow control, a large capacitance will help the system reach the steady-state quickly. To meet the above requirements, a structure of parallel capacitors $C_{10}$ and $C_{11}$ is designed, wherein the value of $C_{10}$ is small and the value of $C_{11}$ is large. During the current flow control, both $C_{10}$ and $C_{11}$ are in the circuit, which gives a large capacitance. Only $C_{10}$ is in circuit during the fault current clearance process. In this study, $C_{10}$ is set as 50 μF and $C_{11}$ is set as 750 μF.

The inductor $L$ is put into the line during the fault current limiting stage to suppress the increase of the fault current. A large inductance would help the suppression but may also have negative impacts on system stability. In a 500 kV HVDC system, the current-limiting inductance has been selected as 0.3 H [19].

## IV. The H-bridge Inter-line CFC with Fault Current Limiting Capability

*A. Topology of the Proposed H-bridge Inter-line CFC*

The proposed CFC requires a large number of IGBTs during the fault current limiting process. Therefore, an H-bridge inter-line CFC uses thyristors is proposed. The topology is shown in Fig. 9. This topology includes H-bridges consisting of thyristors, the current flow control circuit (CFCC), and the fault current limiting circuit (FCLC). The thyristors $T_1$~$T_4$ and $T_5$~$T_8$ form two H-bridges in two lines. The directions of the currents $i_1$ and $i_2$ shown in Fig. 8 are defined as positive directions. The thyristors $T_1$ and $T_2$ ($T_5$ and $T_6$) are turned on if the current of line 1 (line 2) is positive. Otherwise, the thyristors $T_3$ and $T_4$ ($T_7$ and $T_8$) are turned on. In this way, the current flowing through CFCC and FCLC is always positive.

The CFCC consists of four IGBTs ($V_1$~$V_4$) and their series connected diodes, four capacitors ($C_{10}$, $C_{11}$, $C_{20}$, $C_{21}$), inductor $L_{lim}$, four auxiliary bidirectional switches ($V_{1a}$, $V_{2a}$, $V_{1b}$, $V_{2b}$), four ultra-fast disconnectors ($UFD_1$~$UFD_4$), and four bidirectional switches ($S_1$~$S_4$). The FCLC of the two lines shares some components with the CFCC. Except for the four IGBTs ($V_1$ ~ $V_4$) and their diodes, the rest of the devices also belongs to the FCLC. In addition, the FCLC includes 14 thyristors ($T_{1a}$ ~ $T_{7a}$, $T_{1b}$ ~ $T_{7b}$) on two lines.

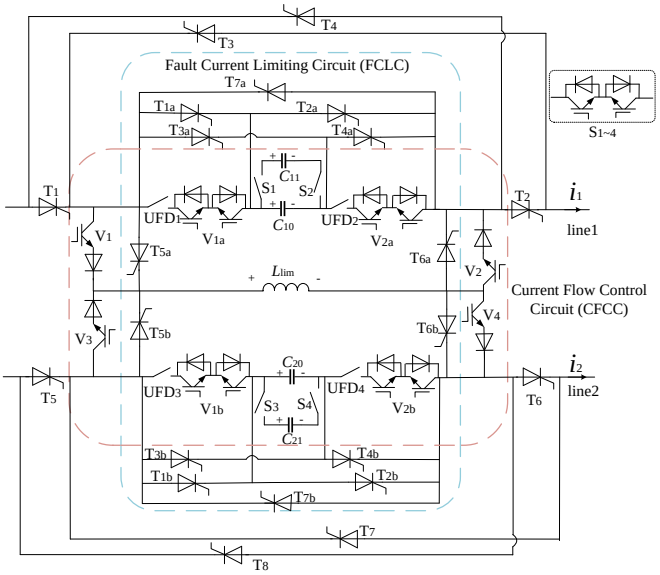


Fig. 9. Topology of the proposed new inter-line CFC.

There are two differences between the second topology and the first one. First, the second topology uses H-bridges which achieve a single current direction of CFCC and FCLC, resulting in the reduce of devices. Second, the latter only uses thyristors in the FCLC without involving IGBTs. The capacitor voltage is used to control the thyristors for current limiting. The proposed inter-line CFC does not have a fault current interrupting capability.

*B. Operating Principle of the Proposed H-bridge Inter-line CFC*

During normal operation, $T_{1a}$ ~ $T_{7a}$, $T_{1b}$ ~ $T_{7b}$ are turned off, $UFD_1$ ~ $UFD_4$ are closed, $V_{1a}$, $V_{2a}$, $V_{1b}$, and $V_{2b}$ are turned on, the two lines are flow-controlled. The principle of current flow control of this CFC is similar to the processes described in Section II, and therefore, is not repeated here.

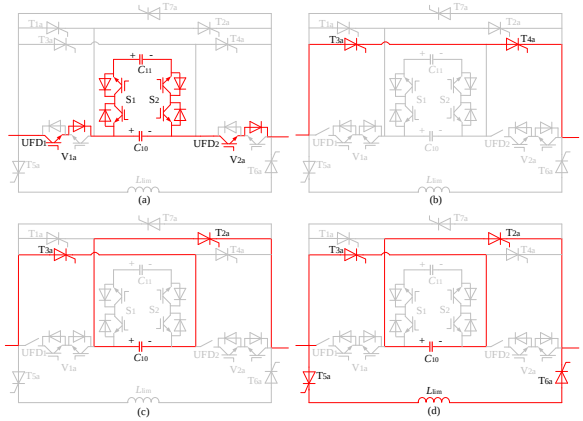


Fig. 10. Operation principle of the fault current limiting. (a) Stage I; (b) Stage II; (c) Stage III; (d) Stage IV.

$V_1$ to $V_4$ are turned off if a pole-to-ground fault occurs in either line. The thyristors are controlled to switch the inductor $L_{lim}$ into fault current limiting. Assuming the fault occurs in line 1 and the currents of lines 1 and 2 are shown in Fig. 9.

There are also two operating conditions as presented in Section II. For the first condition, the fault current limiting processes are shown in Fig. 10 in the case that the voltages of $C_{10}$ and $C_{11}$ are positive. The fault current begins to decay when the DCCB of line 1 operates. Then, the voltage of $L_{\text{lim}}$ reverses, $T_{7a}$ is turned on and the inductor $L_{\text{lim}}$ is bypassed.

## V. Simulation and Verification

### A. Validation of Proposed CFC

#### a. Test in the equivalent circuit

The test circuit shown in Fig. 8 is built in PSCAD/EMTDC V4.5 with a simulation time step of 20 μs. The parameters are given in TABLE II. The fault occurs at $t$ = 0.5 s. The simulation results of the fault current are compared with the analytical calculation conducted in Section III. The results are shown in Fig. 11.

TABLE II
CIRCUIT PARAMETERS

| Parameters | Values |
|---|---|
| $u_{dc}$, $u_0$ [kV] | 500,10 |
| $R_s$, $R_l$, $R_0$ [ Ω ] | 2, 3, 3000 |
| $L_{dc}$, $L_l$, $L$ [mH] | 150, 50, 300 |
| $C_{10}$ [μF] | 50 |
| $I_0$ [kA] | 2 |

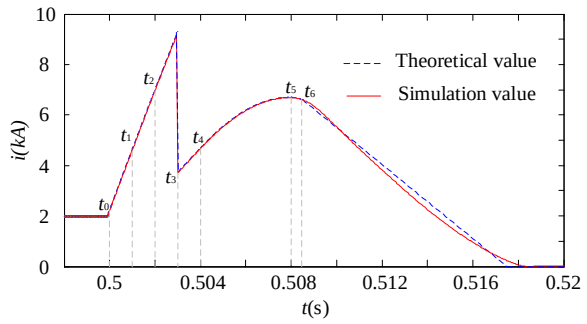


Fig. 11. Comparison between analytical calculation and simulation.

It is seen that the analytical calculation and the simulation match well during the period of $t_0$~$t_6$ before the arrester acts. This verifies the correctness of the theoretical analysis in Section III. There is a slight difference between the two results because of the use of a simplified resistance of the arrester.

#### b. Test in a four-terminal HVDC grid

The parameters of the four-terminal DC grid shown in Fig. 6 and CFC are given in Table III.

1) *DC current flow control*

The current of line1 ($i_{12}$) is controlled to 2.40 kA at $t$ = 2 s. The simulation results are shown in Fig. 12. The voltages and currents changed when the current flow is triggered. Then the system becomes stable. The current $i_{12}$ reaches the target value 0.8 s later with a smooth transient process. The voltages of the converter do not experience large fluctuations. It is seen that the capacitor voltages fluctuate greatly during the transient process. It is because their capacitances are small. However, it has small effects on the overall system operation. The simulation results show that the CFC can control the current flow quickly and stably.

TABLE III
PARAMETERS OF THE FOUR-TERMINAL DC GRID AND CFC

| Transmission Lines Parameters | | | | |
|---|---|---|---|---|
| **Lines** | **Length [km]** | **Resistance [Ω]** | **Reactance [H]** | |
| line1 | 227 | 7.786 | 0.292 | |
| line2 | 66 | 2.264 | 0.085 | |
| line3 | 219 | 7.512 | 0.281 | |
| line4 | 126 | 4.322 | 0.162 | |
| **Converter Parameters** | | | | |
| Bus | 1 | 2 | 3 | 4 |
| Voltage [kV] | - | ±500 | - | - |
| Power [MW] | 750 | - | 1500 | -1500 |
| **CFC Parameters** | | | | |
| $C_{10}$, $C_{20}$ [μF] | | 50, 50 | | |
| $C_{11}$, $C_{21}$ [μF] | | 750 | | |
| $L$ [mH] | | 300 | | |

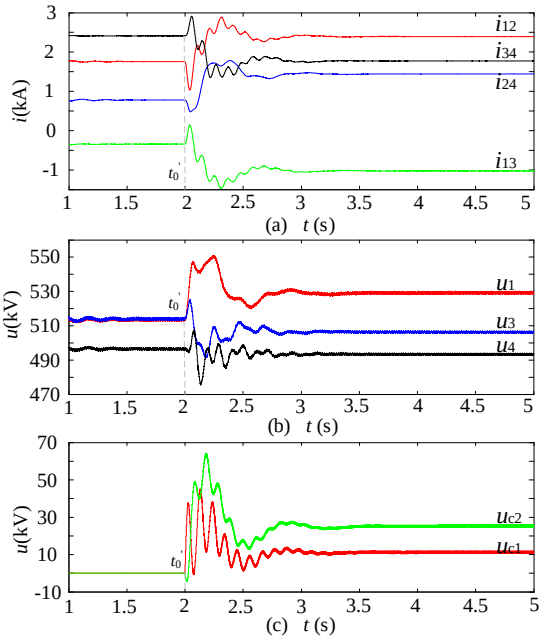


Fig. 12. System responses during the current flow control. (a) Currents; (b) DC voltages; (c) CFC capacitor voltages.

2) *Fault current limiting and clearance*

A pole-to-ground fault occurs on line 1 at $t$ = 5.5 s. Assuming that the protection system takes 1 ms to detect the fault and send out the action signal. The simulation results are shown in Fig. 13. The fault current can be cleared in 18 ms.

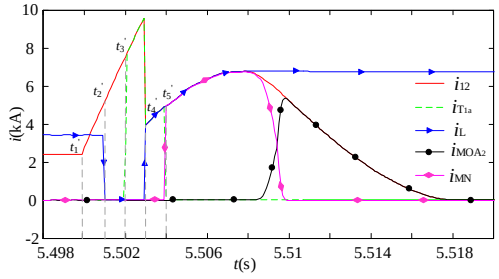


Fig. 13. Results of the fault current limiting and clearance.

To verify the effectiveness of the current limiting, tests have been conducted with and without triggering the current limiting mode. As shown in Fig. 14, the fault current is immediately reduced by 58.87% after triggering the current-limiting mode. The peak fault current is reduced by 27.78% as well. The CFC has good fault current limiting and interrupting capabilities

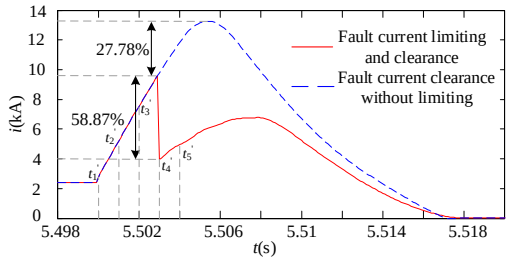


Fig. 14. Verification of current limiting effect.

*c. Comparison with existing methods*

The proposed CFC (Scheme 1) has been compared with the inductor sharing inter-line CFC proposed in [25] and the hybrid FCL proposed in [19] (Scheme 2). The comparison of the two schemes uses the same parameters. Simulation results are shown in Fig. 15.

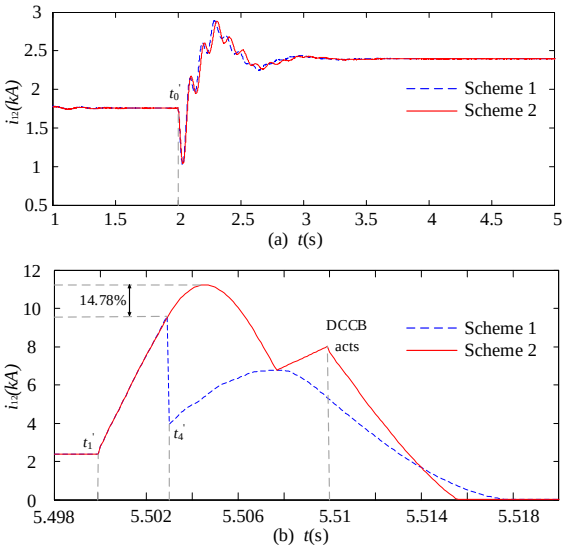


Fig. 15. Comparison of the proposed CFC with the other scheme. (a) Current flow control capability; (b) Fault current limiting and interrupting capability.

It can be seen from Fig. 15(a) that both schemes have excellent performance in current flow control. From Fig. 5(b), the peak current of Scheme 1 is 9.57 kA which is 14.78% lower than Scheme 2's 11.23 kA. Moreover, the fault current under Scheme 1 is still less than Scheme 2 during the current limiting and dissipating periods.

*B. Verification of Proposed H-bridge inter-line CFC*

The proposed H-bridge inter-line CFC is deployed in the DC bus of station 2 of the DC power grid shown in Fig. 6. The parameters of inter-line CFC are: $L_{\text{lim}}$ =300 mH, $C_{10}$=$C_{20}$= 50 mF, $C_{11}$=$C_{21}$= 750 mF. At $t$ = 5 s, a pole-to-ground fault occurs on line 4. FCLC performs and cooperates with DCCB on line 4 to interrupt the fault current. The simulation results are shown in Fig. 16. The fault current can be limited to 7 kA and be cleared in 13 ms.

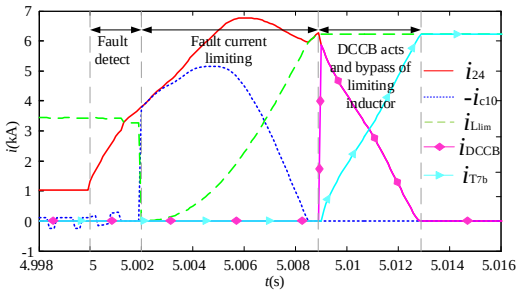


Fig. 16. Currents of the fault current limiting process.

Fig. 17 illustrates the comparison of the fault current in three cases. In case 1, the DCCB acts without fault current limiting. The fault current limiting is triggered but $L_{\text{im}}$ is not bypassed in case 2. In case 3, the fault current limiting and $L_{\text{im}}$ is bypassed when DCCB acts. It is seen that the fault current value is reduced by 43.87% if the $L_{\text{im}}$ is fully put into operation when DCCB operates. It shows the proposed inter-line CFC has a good performance in current limiting. After the inductor $L_{\text{im}}$ is bypassed, the falling rate of the fault current is accelerated. The time taken to clear the fault current is reduced by about 3.6 ms.

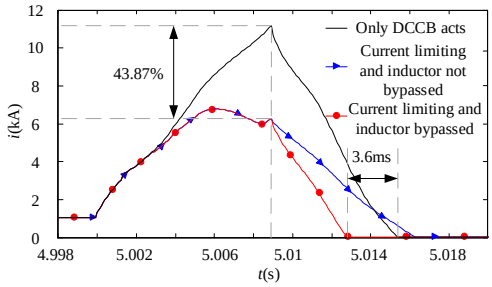


Fig. 17. Comparison of fault currents in three cases.

## VI. Conclusions

In this paper, a CFC with DC fault current limiting and interrupting capabilities has been proposed. The topology, operation process and theoretical analysis are presented. The proposed CFC can perform current flow control on two lines during the normal operation. During the fault clearance process, the capacitor voltage is used to control the switching of thyristors to interrupt the fault current. It can effectively limit the rising rate and the peak value of the DC fault current. In the case of a four-terminal DC grid, the fault current can be reduced by 58.87% and the peak value of the fault current can be reduced by 27.78% compared to the case without using the CFC.

To reduce the use of IGBTs in the proposed CFC, an H-bridge inter-line CFC with fault current limiting capability is proposed. This CFC uses thyristors during fault current

limiting, and bypasses the current-limiting inductor when the DCCB function operates. The fault current value can be reduced by 43.87% when the DCCB function operates. Additionally, the time taken to clear the fault current can be reduced by about 3.6 ms.

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