

# A Multi-Port Current-Limiting Hybrid DC Circuit Breaker

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**Abstract**—Recently the hybrid multi-port DC circuit breaker (MP-DCCB) is becoming popular in protecting HVDC grids, thanks to their reduction of power electronics devices. In this paper, an enhanced multi-port current-limiting DCCB (MP-CLCB) for multiple line protection is proposed. The integrated fault current limiter (FCL) inside the MP-CLCB can clear the fault faster with slightly increased costs. To reduce the energy dissipation requirement for the surge arresters caused by the newly added current-limiting path, an energy transfer path which provides a loop with the inductors during the current decay stage is designed. The theoretical analysis of the pre-charging, current-limiting, fault interruption and energy dissipation of the MP-CLCB is carried out. Moreover, the design principles of the energy dissipation and the key parameters of the MP-CLCB are provided. The proposed approaches are verified through simulations in PSCAD/EMTDC. The results show that the MP-CLCB can replace multiple DCCBs, accelerate the fault current interruption and reduce the energy dissipation requirement for the surge arresters.

**Index Terms**—HVDC grid; multi-port DC Circuit Breaker (MP-DCCB); fault current limiter (FCL); energy dissipation.

## NOMENCLATURE

MP-CLCB	Multi-Port Current-Limiting Circuit Breaker
UFD	Ultra-Fast Disconnecter
LCS	Load Commutation Switch
NCP	Nominal Current Path
MBP	Main Breaker Path
MBU	Main Breaker Unit
CLP	Current-Limiting Path
CPP	Capacitor Pre-charging Path
ETP	Energy Transfer Path

## I. INTRODUCTION<sup>1</sup>

Recently, the modular multilevel converter (MMC) based high voltage direct current (HVDC) grid, which is formed by interconnecting multiple converter stations, is becoming

popular due to their flexible operation and control in achieving a high penetration of renewable energy [1]-[3]. However, a DC grid has low inertia and impedance at the DC side, which results in its fast dynamic response [4]. DC fault currents may increase quickly following a DC short-circuit in the HVDC grid, which may damage the converters and other equipment.

Compared to the DC fault ride-through scheme using MMCs with self-blocking sub-modules (SMs), the DC circuit breaker (DCCB) based protection can ensure the selectivity of clearing the DC fault and a fast system restoration [5]-[7]. Hence, DCCBs may have a broad prospect in HVDC grids. Hybrid circuit breakers (HCBs) have lower on-state losses than solid-state DCCBs and faster fault current interrupting speed than mechanical DCCBs [8]-[9]. One of the classical configurations is ABB's HCB which consists of two paths: the nominal current path (NCP) and main breaker path (MBP) [10]. However, the extensive capital cost will be the bottleneck if DCCBs are installed at all lines connecting to a common DC bus [11].

Integrating the HCBs into one multi-port DCCB (MP-DCCB) can reduce the use of power electronic devices [12]-[15]. An interlink HCB for unidirectional and bidirectional interruption has been proposed in [12], which features its reduced sizes and costs. In [13], an integrated DCCB for meshed HVDC grids has been proposed, wherein the breakers connected to the same DC bus are merged into the proposed integrated DCB. However, they do not have the current limiting capability. The MP-DCCB in [14] utilizes the characteristics of HCB and reduces the number of components. However, overcurrent may be observed when the fault current flows through the lower arm of the faulty line. The MP-DCCB proposed in [15] embeds current limiting inductors and can effectively limit the rate-of-change of the DC fault currents. However, the remaining energy in the inductor may slow down the decay of the fault current and increase the energy dissipated by surge arresters (SAs).

It may take several milliseconds for MP-DCCB to interrupt the fault current. The rapid development of fault current may result in a large overcurrent. A fault current limiter (FCL) can limit the rate-of-change of the fault current and therefore, reduce the burden of DCCBs. The FCL based on power electronics devices can be classified into solid and hybrid categories [16], [17]. The solid FCL has high on-state losses and limited capacity. The hybrid FCL combines the advantages of power electronics and mechanical switches. Thanks to their fast development, hybrid DCCBs with current limiting capability are emerging. Reference [18] proposes an HCB that has different current limiting function for protecting permanent

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and temporary DC faults. However, this type of DCCB can only operate in low voltage DC systems.

The paper proposes a novel topology of the multi-port current-limiting DCCB (MP-CLCB) which combines the multi-port DCCB and FCL. The current-limiting path (CLP) uses high rating thyristors which are durable and economical as the main switch. The free-wheeling path proposed in [19] has been employed to accelerate the current decay in the SA. In the proposed MP-CLCP, an energy transfer path (ETP) by adding additional thyristors and capacitor to the path is employed to bypass the inductors and accelerate the fault current decay. The current commutation path in the proposed MP-CLCB shares the similar concept with ABB's hybrid breaker [20]. The main innovation of the proposed topology is to enhance the performance of such type of hybrid breakers through proposing the current limiting path which can reduce the fault current and the ETP which can dissipate energy in inductors [21]-[22]. In this case, the shunt columns of SA can be reduced, which is beneficial to the manufacture and its cost. Moreover, reducing the dissipated energy of the SA is very important to reduce the shunt columns of SA and therefore, will be beneficial to the manufacture and its cost. The operation principle of the proposed MP-CLCB is provided and its effectiveness is verified through simulations in PSCAD/EMTDC.

## II. TOPOLOGY AND OPERATIONAL MECHANISM OF THE PROPOSED MP-CLCB

### A. Existing Multi-Port DCCB

Fig. 1 shows the topologies and configurations of the conventional DCCB and the existing MP-DCCB [14] in a DC grid. It is shown that an MP-DCCB protects  $n$  lines connected to the same DC bus.

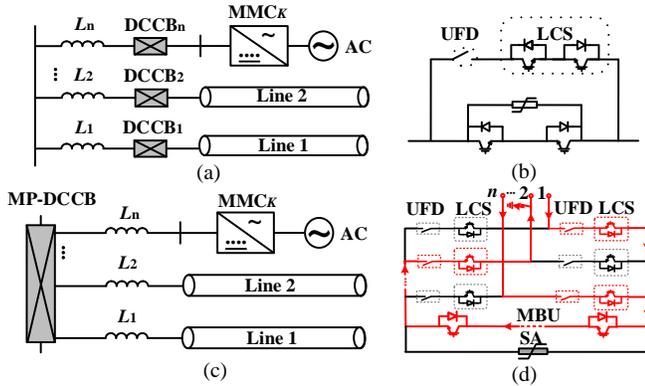


Fig. 1. Configuration of DCCBs and the MP-DCCB: (a) deployment of conventional DCCBs; (b) topology of the conventional HCB; (c) deployment of the MP-DCCB; (d) topology of existing MP-DCCB.

The current transfer process of the MP-DCCB [14] installed in Fig. 1(c) is shown in Fig. 1(d) in case of a fault in Line 2. During normal operation, current flows through both the upper and lower arms, which is equivalent to a parallel connection of the upper and lower arms. Thus, the on-state losses are less than the conventional DCCB. However, due to the lack of current-limiting capability, similar to the HCB, the

MP-DCCB needs to interrupt a large fault current. To handle this issue, a DCCB with embedded FCL has been proposed in [20], which can limit the rate-of-change of the fault current and therefore, reduce the energy dissipated in the SA and the interruption time.

### B. Topology of the Proposed MP-CLCB

The proposed MP-CLCB is shown in Fig. 2. The breaker consists of two main parts: the NCP and the main branch shared by all connected branches. Each NCP consists of an ultra-fast disconnecter (UFD) and a load commutation switch (LCS). The UFD and diodes with large current ratings are connected between each NCP and the main branch. The main branch is composed of an MBP, a CLP, a capacitor pre-charging path (CPP) and an ETP.

The function of each path is: **CPP**- Charging capacitor  $C_{CLP}$ , which is required for current commutation among branches during current interruption; **ETP**- Improving dissipation energy in  $L_{dci}$  and  $L_{FCL}$  when the main breaker unit (MBU) is turned off; **MBP**- Commutating and interrupting fault current to help  $UFD_i$  and  $LCS_i$  turn off; **CLP**- Commutating current into the current-limiting inductor  $L_{FCL}$ .

The CPP, which is composed of resistor  $R_g$ , capacitor  $C_g$  and thyristor  $T_{g_2}$ , is to pre-charge the high-voltage capacitor under the DC voltage. As  $C_{CLP}$  and  $C_g$  will remain charged for a long time, resistive grounding preventing leakage currents is needed to clamp their voltages. The thyristor  $T_{g_2}$  is applied to discharge  $C_g$  through the  $R_g$ . The utilization of  $T_{g_2}$  might increase cost and size. However, the size and cost can be minimized by optimizing the system dimension and design.

The ETP consists of three parts: 1) Thyristor  $T_d$ , which is used to form a loop with the inductor. 2) Pre-charged capacitor  $C_{ETP}$ , whose discharging process provides a reversed turn-off voltage for  $T_d$ . Before operation,  $C_{ETP}$  will be pre-charged to about 1 kV through a power source, e.g. the laser energy charging technology. 3) Resistor  $R$ , which absorbs the energy of the capacitor. The MBP consists of an IGBT group and a SA group.

The CLP has three parts: 1) The thyristor valve group  $T_a$ , which is used to rapidly transfer the fault current to ensure the UFD can open at zero current. 2) The branch with parallel connected  $T_b$  and  $T_{g_1}$ , and the pre-charging capacitor  $C_{CLP}$  with a paralleled surge arrester, which overall ensures the turn-off of  $T_a$ . Moreover, the reverse charging of the capacitor can store partial energy and limit the rate-of-change of the current. 3) The branch with the thyristor valve group  $T_c$  and the current limiting inductor  $L_{FCL}$ . As the line current limiting inductor  $L_{dci}$  ( $i=1, 2, \dots, n$ ) may affect the dynamic characteristics of the DC system,  $L_{FCL}$  will not be inserted into the circuit during normal operation and will be inserted into the main path to suppress fault currents.  $L_{FCL}$  is used to limit the rate-of-rise of the fault current and therefore, reduce the voltage-of-rise of the capacitor  $C_{CLP}$ . In fact, the MP-DCCB could operate without  $L_{FCL}$ , as many DCCBs with parallel capacitors have been reported in the open literature. However, the DCCB without the FCL may cause overvoltage on  $C_{CLP}$ . To avoid the overvoltage, the capacitance of the  $C_{CLP}$  should be increased. However, this solution would in turn increase the volume and





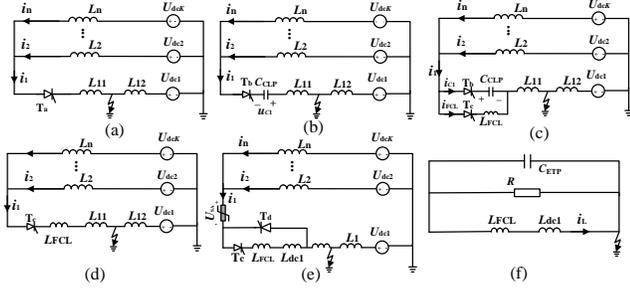


Fig. 6. Equivalent circuits during the current interrupting process: (a)  $t_0 \sim t_1$ , (b)  $t_1 \sim t_2$ , (c)  $t_2 \sim t_3$ , (d)  $t_3 \sim t_4$ , (e)  $t_4 \sim t_5$ , (f)  $t_5 \sim t_6$ .

The stage-by-stage equivalent circuits during the fault interruption process are shown in Fig. 6.

In Fig. 6,  $L_i$  ( $i=2, 3, \dots, n$ ) is the sum of all inductances between the near converter to the remote DC bus. It includes the equivalent inductance of  $MMC_K$ , inductance of  $L_{dci}$ , and the equivalent line inductance of the lumped parameters of the transmission line model.  $L_{11}$  is the equivalent inductance from the fault point to the remote DC bus.  $L_{12}$  is the equivalent inductance from the fault point to the  $MMC_K$ .  $L_{FCL}$  is the inductance of CLP, and  $L_{dcl}$  is the line current limiting inductor. Each converter station is equivalent to a DC voltage source whose voltage is  $U_{dci}$  ( $i=1, 2, \dots, K$ ). Resistance of converters and lines, and the on-state voltage drop of each power electronics device are ignored as they are relatively small.

#### a. Analysis of stage I

During the steady-state,  $T_g$  and  $T_{g1}$  are on and the DC grid pre-charges the commutation capacitor. The thyristor is automatically turned off once the current drops to zero and the pre-charging process ends. The initial pre-charging voltage  $u_{10}$  can be adjusted by setting the parameter of  $C_g$ :

$$u_{10} = \frac{C_g}{C_g + C_{CLP}} u_{dc} \quad (1)$$

#### b. Analysis of stage II

##### 1) $t_0 \sim t_2$

During the period of  $t_0 \sim t_2$ , the fault current continues to rise through  $T_a$  in CLP, as is shown in Fig. 6(a). The steady-state current of the faulty DC Line 1 is denoted as  $I_{1N}$ . Based on KCL and KVL, the fault current  $i_1$  is expressed as:

$$i_1 = I_{1N} + \frac{\Sigma_2}{1 + L_{11}\Sigma_1} (t - t_0) \quad (2)$$

where  $\Sigma_1$  and  $\Sigma_2$  are defined as:

$$\begin{cases} \Sigma_1 = \sum_{j=2}^n 1/L_j \\ \Sigma_2 = \sum_{j=2}^n U_{dcj} / L_j \end{cases}$$

##### 2) $t_2 \sim t_3$

At  $t_2$ , the capacitor  $C_{CLP}$  begins to discharge, and the faulty line current will be quickly transferred from  $T_a$  to  $C_{CLP}$ . The equivalent circuit diagram is shown in Fig. 5(b). The dynamic process of  $C_{CLP}$  discharge is described as:

$$\begin{cases} U_{dcj} = L_j \frac{di_j}{dt} - u_{C_{CLP}} + L_i \frac{di_i}{dt} \quad (j=1 \dots n, j \neq i) \\ i_i = -C_{CLP} \frac{du_{C_{CLP}}}{dt} \\ i_i = \sum_{j=1, j \neq i}^n i_j \end{cases}$$

Ignoring the time that the current through  $T_a$  drops to zero, and assuming that the current is transferred to the commutating capacitor immediately at  $t_2$ . Substituting  $t_2$  into (2), it is obtained that  $i_{C_{CLP}}(t_2) = i_1(t_2) = I_2$ , then

$$\begin{cases} u_{C_{CLP}} = \sqrt{A_1^2 + B_1^2} \sin(\beta(t - t_2) + \varphi_1) + D_1 \\ i_i = -\beta C_{CLP} \sqrt{A_1^2 + B_1^2} \cos(\beta(t - t_2) + \varphi_1) \end{cases} \quad (3)$$

where all the variables are defined as:

$$\begin{cases} \beta = \sqrt{\Sigma_1 / C_{CLP} (1 + L_{11}\Sigma_1)} \\ A_1 = \Sigma_2 / \Sigma_1 + U_0 \\ B_1 = -I_2 / C_{CLP} \beta \\ \tan \varphi_1 = A_1 / B_1 \\ D_1 = -\Sigma_2 / \Sigma_1 \end{cases}$$

When designing the initial voltage and capacitance of the capacitor, the discharging process of (3) should be considered to ensure that  $u_{C_{CLP}} > 0$ . This is to make sure that the reversed voltage is continuously applied on  $T_a$  until it is completely turned off.

##### 3) $t_3 \sim t_4$

At  $t_3$ ,  $u_{C_{CLP}} = 0$ , the reverse charging of  $C_{CLP}$  starts, then  $T_c$  is turned on due to the forward voltage. The equivalent circuit diagram is shown in Fig. 6(c). The initial conditions are  $u_{C_{CLP}}(t_3) = 0$ ,  $i_{C_{CLP}}(t_3) = i_1(t_3) = I_3$ , based on KVL, then:

$$\begin{cases} u_{C_{CLP}} = \xi \sin(\gamma(t - t_3) + \varphi_2) - A_2 \\ i_{C_{CLP}} = -\gamma C_{CLP} \xi \cos(\gamma(t - t_3) + \varphi_2) \\ i_{FCL} = (\xi \sin(\gamma(t - t_3) + \varphi_3) + A_2 \gamma(t - t_3) + B_2) / L_{FCL} \gamma \\ i_i = i_{C_{CLP}} + i_{FCL} \end{cases} \quad (4)$$

where variables are defined as:

$$\begin{cases} A_2 = \Sigma_2 / [(L_1 \Sigma_1 + 1) / L_{FCL} + \Sigma_1] \\ B_2 = I_3 / C_{CLP} \gamma \\ \xi = \sqrt{A_2^2 + B_2^2} \\ \tan \varphi_2 = A_2 / B_2 \\ \tan \varphi_3 = -B_2 / A_2 \\ \gamma = \sqrt{\frac{1}{C_{CLP}} \left( \frac{1}{L_{FCL}} + \frac{1}{C_{CLP} (1 / \Sigma_1 + L_{11})} \right)} \end{cases}$$

##### 4) $t_4 \sim t_5$

As  $C_{CLP}$  is charged,  $u_{C1}$  will gradually increase, and  $i_{C1}$  will

gradually decrease. When  $u_{C1}$  equals the system voltage, the line current begins to decrease, and  $u_{C1}$  will gradually rise above the system voltage. At  $t_4$ ,  $i_{C1}=0$ ,  $C_{CLP}$  is charged to the highest voltage,  $T_b$  turns off and the capacitor is thus disconnected.

After  $t_4$ , the fault current completely flows through the current limiting inductor, based on (4),  $i_1(t_4)=I_4$ . The equivalent circuit diagram is shown in Fig. 6(d). After  $t_4$ , the faulty current  $i_1$  is expressed as:

$$i_1 = I_4 + \frac{\Sigma_2}{1 + (L_{11} + L_{FCL})\Sigma_1} (t - t_4) \quad (5)$$

Compared with (2), the insertion of the current limiting inductor reduces the rate-of-rise of the DC fault current.

### c. Analysis of stage III

At  $t_5$ , the MBU is turned off, and the  $T_d$  of ETP is turned on. When SA operates, and the fault current is gradually reduced. At time  $t_6$ , the fault current drops to zero, and the decay time of current is defined as  $\Delta t_{\text{break}}$ .

The faulty line current  $i_1(t_5)=I_5$  can be obtained from (5), and the voltage during the operation of the SA is  $U_{SA}$ . During the decay of current:

$$i_1 = I_5 + \frac{\Sigma_2 - \Sigma_1 U_{SA}}{1 + (L_{11} - L_{dc1})\Sigma_1} (t - t_5) \quad (6)$$

$$\Delta t_{\text{break}} = I_5 \cdot \frac{1 + (L_{11} - L_{dc1})\Sigma_1}{\Sigma_1 U_{SA} - \Sigma_2} \quad (7)$$

The energy that the SA needs to be dissipated is:

$$E_{SA} = \frac{I_5^2 U_{SA}}{2} \cdot \frac{1 + (L_{11} - L_{dc1})\Sigma_1}{\Sigma_1 U_{SA} - \Sigma_2} \quad (8)$$

The equivalent circuit is shown in Fig. 6(e). When the current begins to decay,  $I_5$  is smaller than that without CLP. As can be seen from (7) and (8), the reduction of  $I_5$  reduces the interruption time and energy dissipation of SA. Additionally, the ETP forms a loop with the inductors which results in the reduction of the interruption time and dissipated energy.

### d. Analysis of stage IV

At  $t_6$ , the capacitor  $C_{ETP}$  of ETP starts to discharge. Ignoring the time that  $T_d$ 's current drops to zero, then the DC inductor current is immediately transferred to the commutation capacitor at time  $t_6$ . It is obtained that  $i_{C2}(t_6)=i_1(t_6)=I_5$ ,  $u_{CETP}(t_6)=-u_{CETP,pre}$ ,  $L_d=L_{dc1}+L_{FCL}$ , the time interval from  $t_6$  to the time when the voltage is zero at  $t_7$  is  $\Delta t_{OFF}$ , and the time interval from  $t_6$  to  $t_8$  when the inductor current decays to zero is  $\Delta t_{att}$ . According to the equivalent circuit diagram shown in Fig. 6(f), it can be obtained:

$$\left\{ \begin{array}{l} i_L(t) = I_5 \cos \frac{t-t_6}{\sqrt{C_{ETP}L_d}} + u_0 \sqrt{\frac{C_{ETP}}{L_d}} \sin \frac{t-t_6}{\sqrt{C_{ETP}L_d}} \\ u_{C_{ETP}}(t) = I_5 \sqrt{\frac{L_d}{C_{ETP}}} \sin \frac{t-t_6}{\sqrt{C_{ETP}L_d}} - u_0 \cos \frac{t-t_6}{\sqrt{C_{ETP}L_d}} \\ \Delta t_{OFF} = \sqrt{C_{ETP}L_d} \tan^{-1} \left( \frac{u_0}{I_2} \sqrt{\frac{C_{ETP}}{L_d}} \right) \\ \Delta t_{att} = \sqrt{C_{ETP}L_d} \left( \pi + \tan^{-1} \left( -\frac{I_2}{u_0} \sqrt{\frac{L_d}{C_{ETP}}} \right) \right) \end{array} \right. \quad (9)$$

The total energy stored in inductors is:

$$W_L = \frac{1}{2} L_d I_5^2 \quad (10)$$

At  $t_7$ ,  $u_{C2}=0$ , the discharge of  $C_{ETP}$  is completed. Then, the DC reactor starts to reversely charge the capacitor. When designing the initial voltage and capacitance of the capacitor, discharge process based on (9) needs to be considered. The interval  $\Delta t_{OFF}$  from  $t_6$  to  $t_7$  needs to be greater than the turn-off time of the thyristor to ensure that  $u_{C2}$  is over zero until  $T_d$  is turned off.

At  $t_8$ , the inductor current drops to zero,  $D_1'$  turns off and the capacitor  $C_{ETP}$  voltage rises to the maximum value. Then the resistor dissipates the residual energy. According to (9) and (10), the smaller the capacitance, the shorter the charging time and the faster the DCCB recovers. However, the maximum voltage across the capacitor increases accordingly. Hence, the capacitor parameters need to be properly designed.

### B. Analysis of Voltage Stress

For each power electronic device, the LCS and the diodes are connected in series with the UFD, so the voltage is small. The maximum voltage  $U_{T_{a\max}}$  of  $T_a$  is the forward voltage, which is equal to  $U_{C1\max}$  of  $C_{CLP}$ . The maximum voltage  $U_{T_{b\max}}$  of  $T_b$  is the reversed voltage which is equal to the total voltage of  $U_{C1\max}$  and the voltage across the current-limiting inductor. The voltage of  $T_c$  is small. The voltage across the MBU is up to the value of  $U_{SA}$ . Specifically:

$$U_{T_{a\max}} = -U_{C1\max} = -u_C(t_4) \quad (11)$$

$$U_{T_{b\max}} = \left| U_{C1\max} + \frac{L_{FCL}(\Sigma_2 - \Sigma_1 U_{SA})}{1 + (L_{11} - L_{dc1})\Sigma_1} \right| \quad (12)$$

The voltage of ETP mainly depends on the inductance and capacitance. The maximum voltage  $U_{TD\max}$  of  $T_d$  is equal to the maximum voltage of the capacitor  $C_{ETP}$ , then

$$U_{C_{2\max}} = u_{C_2}(t_8) = I_5 \sqrt{\frac{L_d}{C_2}} \sin \frac{t_8-t_6}{\sqrt{C_2 L_d}} - u_0 \cos \frac{t_8-t_6}{\sqrt{C_2 L_d}} \quad (13)$$

Using the above equations, the next section will analyze the voltage and current stresses of the proposed MP-CLCB under specific parameters.

## IV. PARAMETER DESIGN AND ECONOMIC ANALYSIS

A  $\pm 500$  kV four-terminal bipolar HVDC grid using half-bridge MMCs shown in Fig. 7 is used for the test. Eight MP-

CLCBs are deployed.  $L_{dci}(i=1, 2, \dots, n)=L_{FCL}=0.15$  H.  $C_{CLP}=10$   $\mu$ F. The line inductance is 1.287 mH/km. The grid parameters are shown in Fig. 7. The  $t_{det}=1$  ms is the fault detection time,  $t_{UFD}=2$  ms is the action time of UFD, and  $T_{off}=60$   $\mu$ s is the turn-off time for  $T_a$  and  $T_d$ .

From the view of MP-CLCB1, the rated current of Line 12 is the largest among the three lines. The pole-to-pole fault marked in Fig. 7 is simulated.  $I_{12N}$  represents the pre-fault current of line 12, substituting DC grid parameters into the power flow calculation, it is obtained that:  $U_{dc1}=512$  kV,  $U_{dc2}=501$  kV,  $U_{dc3}=514$  kV,  $U_{dc4}=500$  kV,  $I_{12N}=1.78$  kA.

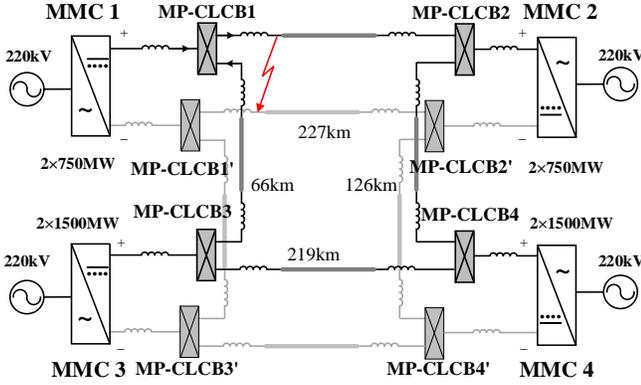


Fig. 7. Test system and locations of MP-CLCBs.

The number of IGBTs in MBP is determined by the maximum voltage and current. The 4.5 kV/3 kA high-power IGBT devices are selected. It is known from (7) and (8) that the larger the  $U_{SA}$ , the faster the current interruption and the smaller the energy dissipation of SA. However, the larger the  $U_{SA}$ , the more IGBTs are needed. In this paper, it is given that  $U_{SA}=800$  kV. Considering 10% of voltage margin, the number of IGBTs in series for MBP is 196.

At  $t=t_0=0$  s, the fault occurs. The time interval from  $t_0$  to  $t_3$  is the sum of  $t_{det}$ ,  $t_{UFD}$  and  $T_{off}$ , i.e.,  $t_3=t_0+t_{det}+t_{UFD}+T_{off}=3.6$  ms. The capacitor discharge process has little effect on the fault current. Substituting  $t_0$ ,  $t_3$  and  $I_{12N}$  into (2), it is calculated that  $I_3=6.23$  kA. Substituting  $I_3$  to (4) and (5), it is obtained that  $I_5=5.82$  kA. As the surge rating for a duration in the single digit millisecond range can be expected upwards 20 kA, the number of IGBTs in parallel with MBP is 1.

For DCCBs and MP-DCCBs, the required numbers of IGBTs are determined by the maximum current and voltage [24]. For both DCCBs and MP-DCCBs, the maximum voltage is 800 kV which is the same as MP-CLCB. The fault current calculated from (2) indicates that the current reaches the maximum value of 8.93 kA at time  $t_5$ . Considering the margin, the number of parallel IGBTs (4.5 kV/3 kA) is 1 and the number in series is 196. Therefore, the MBP of MP-DCCB needs  $1 \times 196$  IGBTs. Taking the reversed fault current direction into consideration, the number of IGBTs for MBP of the DCCB is  $1 \times 196 \times 2 \times n$ . Moreover, as shown in Fig. 1, a DCCB needs  $n$  UFDs and  $2n$  LCSs, and a MP-DCCB needs  $2n$  UFDs and  $2n$  LCSs, where  $n$  is the branch number. The above comparison of the required IGBTs of each topology is given in Table I.

TABLE I  
COMPARISON OF REQUIRED IGBTs

Items		DCCB	MP-DCCB	MP-CLCB
NCP	Parallel	$3 \times n$	$2 \times 3 \times n$	$3 \times n$
	Series	$2 \times 3$	3	3
MBP	Parallel	$1 \times n$	1	1
	Series	$196 \times 2$	196	196
In total		$410n$	$196+18n$	$196+9n$

Compared with the conventional DCCB, the number of IGBTs saved by MP-CLCB is  $401n-196$ . When  $n=2$ , the number of IGBTs is saved by 75.56%. When  $n=3$ , the number of IGBTs is saved by 81.87%. Compared with the MP-DCCB proposed in [14], the number of IGBTs saved is  $9n$ . When  $n=2$ , the number of IGBTs is saved by 7.76%. When  $n=3$ , the number of IGBTs is saved by 10.80%, this comes at the cost of additional components.

According to (9), the value of  $C_{ETP}$  and the pre-charge voltage  $u_{cETP,pre}$  will affect the capacitor discharge time  $\Delta t_{OFF}$ , the current-limiting inductor current decay time  $\Delta t_{att}$ , the thyristor maximum voltage  $U_{Tdmax}$ , the current-limiting inductor current  $i_L$ , and the capacitor voltage  $u_c$ . In order to visually show the influence of the two parameters, firstly,  $C_{ETP}$  is set as 500  $\mu$ F. Based on (9) and (13), the variations of each item under different values of  $u_{cETP,pre}$  is shown in Fig. 8.

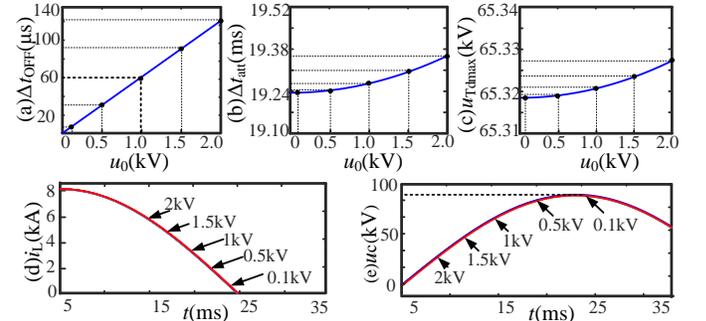


Fig. 8. Effect of  $u_{cETP,pre}$ : (a)  $\Delta t_{OFF}$ : time of the capacitor discharging, (b)  $\Delta t_{att}$ : decay time of inductor current, (c)  $U_{Tdmax}$ : maximum voltage of the thyristor  $T_d$ , (d)  $i_L$ : the current-limiting inductor current, (e)  $u_c$ : the capacitor voltage.

Figs. 8(a) to (c) illustrate the variation of  $\Delta t_{OFF}$  (discharge time of capacitor),  $\Delta t_{att}$  (decay time of inductor's current),  $U_{Tdmax}$  (maximum voltage of the  $T_a$ ) with the pre-charge voltage  $u_{cETP,pre}$ . Figs. 8(d) and (e) show  $i_L$  (current of inductor) and  $u_c$  (voltage of the capacitor) when  $u_{cETP,pre}$  is 0.1, 0.5, 1.0, 1.5 and 2.0 kV.  $\Delta t_{OFF}$ ,  $\Delta t_{att}$  and  $U_{Tdmax}$  increase with the increase of  $u_{cETP,pre}$ . As  $i_L$  and  $u_c$  are less affected by the pre-charge voltage, the time for  $T_d$  to turn off plays a major role. Since  $T_{OFF}=60$   $\mu$ s, the capacitor discharge time is at least 60  $\mu$ s, from Fig. 8(a),  $u_{cETP,pre}$  needs to be over 1.0 kV.

Given that  $u_{cETP,pre}$  is 2.0 kV, the values of each item are calculated based on (5), then the effect of  $C_{ETP}$  is shown in Fig. 9. Figs. 9(a) to (c) illustrate that the variation of  $\Delta t_{OFF}$ ,  $\Delta t_{att}$ ,  $U_{Cmax}$  (the maximum voltage of the capacitor) varies with the value of capacitor  $C_{ETP}$ . Figs. 9(d) and (e) visually show that the development of  $i_L$  and  $u_c$  when the capacitor value is 100, 200, 300, 400 and 500  $\mu$ F. As the capacitance increases,  $\Delta t_{OFF}$  and  $\Delta t_{att}$  increase. Therefore,  $C_{ETP}$  cannot be too large.

However, as the capacitance value decreases,  $U_{C_{max}}$  increases, and the requirement of the voltage capability of  $T_d$  and  $C_{ETP}$  increases. Based on Fig. 9(c), the smaller the capacitance value, the larger increase rate of the maximum voltage will be. Therefore, the capacitance value should be selected in the range of 250-350  $\mu\text{F}$ .

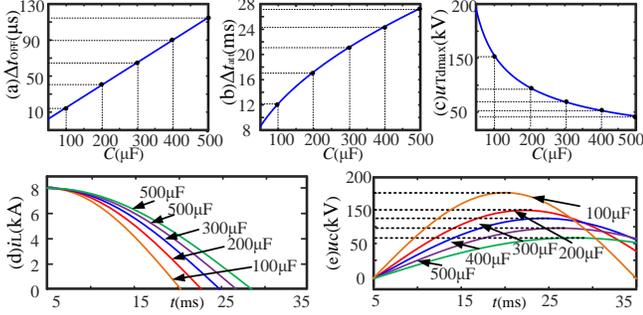


Fig. 9. Effect of  $C_{ETP}$ : (a)  $\Delta t_{OFF}$ : time of the capacitor discharging, (b)  $\Delta t_{fatt}$ : decay time of inductor current, (c)  $U_{T_{dmax}}$ : maximum voltage of the  $T_d$ , (d)  $i_L$ : the current-limiting inductor current, (e)  $u_c$ : the capacitor voltage.

In this paper, the capacitance of  $C_{ETP}$  is 300  $\mu\text{F}$ , the pre-charge voltage  $u_{cETP,pre}$  is 2 kV, and the maximum current of ETP is close to the initial value of  $I_5$ . At time  $t_7$ , the inductor current drops to 0,  $D_1$  turns off, and the voltage of  $C_{ETP}$  rises to the maximum value. Substituting the parameters into (9) and (13), the maximum current of the energy transfer path is 5.83 kA and the maximum voltage is 165.3 kV.

Further, according to (8) and (10), when the current is interrupted, the energy that the SA dissipates is about 10.97 MJ. The energy that ETP absorbs is 29.05 MJ. It indicates that the proposed MP-CLCB reduces the SA capacity by 72.59%. As the large capacity of SA requires a large number of insulator columns in series and parallel, the problem of voltage and current equalization in the complex electromagnetic transient process is one of the bottlenecks [22] that limit the capacity increase of the SA. Moreover, the introduction of the energy transfer path can effectively extend the service life of the SAs. It can be seen that, compared with the existing MP-DCCB proposed in [14], the MP-CLCB not only saves the number of IGBTs but also effectively reduces the capacity of the SA at the cost of additional components.

For  $D_1'-D_n'$  and  $D_1-D_n$ , the diode model is D2601N90T whose rated voltage is 9 kV and design voltage is 4.5 kV. For CLP and ETP, 5STB18U6500 thyristor is adopted in MP-CLCB [25]. Its rated voltage and current are 6.5 kV and 1.5 kA. It can withstand 29 kA maximum surge current for not more than 10 ms. Taking the voltage margin into account, the design voltage of the thyristor is 3.25 kV [12]. As is given in Table II, the number and requirement of each component are given based on its voltage and current need to withstand.

Components	Voltage	Current	Number	Total
$D_1'-D_n'$	10 kV	6.2 kA	$3n$	Diode
$D_1-D_n$	10 kV	5.8 kA	$3n$	$6n$
$T_a$	750 kV	6 kA	230	Thyristor 263
$T_b$	20 kV	6.2 kA	6	
$T_c$	20 kV	6.2 kA	6	
$T_d$	65.3 kV	6.2 kA	20	
$T_e$	2 kV	5.8 kA	1	
$C_{CLP}$	Value: 50 $\mu\text{F}$ ; Voltage requirement: 750 kV.			
$C_{ETP}$	Value: 300 $\mu\text{F}$ ; Voltage requirement: 165.3 kV.			
$R$	Energy dissipation requirement: 31.05 MJ.			

## V. SIMULATION AND VERIFICATION

The system shown in Fig. 7 is used in the simulation, the parameters and scenarios are the same as Section III.

### A. Verification of Current Suppression

Currents of the lines connected to the MP-CLCB1 are shown in Fig. 10. In steady state, MMC2 and MMC3 work in the rectifier mode, and MMC1 receives power. As the healthy Lines 2 and 3 are far away from the fault point, the fault current rises slowly. Therefore, the currents of Lines 2 and 3 are only slightly limited by using MP-CLCB. The current of Line 1 is cleared after effective fault current limiting. Fig.10 shows 3 cases: (a) the MP-CLCB operates; (b) only the circuit breaker operates without triggering the current limiting function; (c) the circuit breaker does not operate. Compared with the case where the circuit breaker does not operate, the fault is cleared very fast. Compared with the case where only the circuit breaker operates, the maximum value of the fault current is reduced.

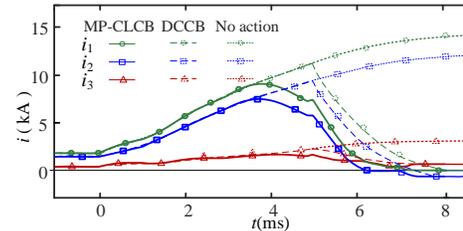


Fig. 10. Line currents of MP-CLCB ports.

The currents flow through the paths of the MP-CLCB and the voltage of main components are shown in Fig. 11. At time  $t_0=1.5\text{s}$ , the fault occurs, and the fault line current  $i_1$  rises rapidly. After 1 ms,  $T_a$  and the IGBTs of the main breaker path are turned on. After a delay of 100 $\mu\text{s}$ , at time  $t_1=1.1$  ms,  $LCS_1$  is turned off, the current in  $LCS_1$  drops rapidly. At time  $t_1=1.2$  ms, the current is less than the residual current of the corresponding UFD, and  $UFD_1$  starts to open. The red dotted line in Fig. 11 shows that the results calculated in MATLAB match well with the simulation results. It can be seen from Fig.11(e) that, after the fault has been cleared, the system will recover to a new steady state in about 150 ms which is faster than the case where only the regular DCCB operates. Fig.11(f) shows the voltage of  $C_{CLP}$ , the voltage that  $C_{CLP}$  needs to withstand is about 750 kV. Fig.11(g) shows the voltage of  $C_{ETP}$ , when the current in the inductor drops to 0, the voltage of  $C_{ETP}$  is the largest, about 165.3 kV.

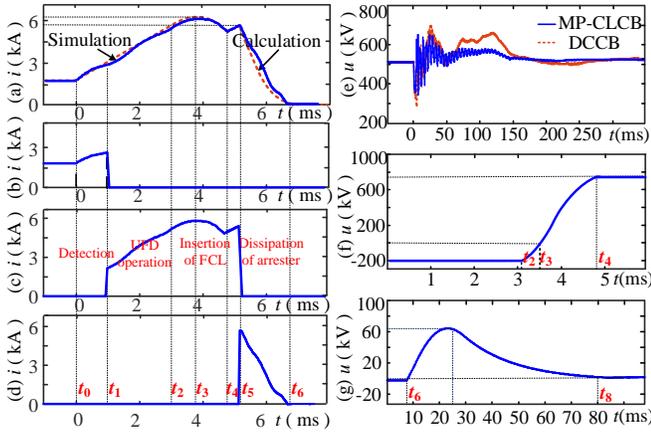


Fig. 11. Current and voltage of main components of MP-CLCB: (a) Line 1, (b) NCP, (c) MBU, (d) SA, (e) DC Bus, (f)  $C_{CLP}$ , (g)  $C_{ETP}$ .

### B. Verification of Current Decay Process

The current of the inductors and the capacitor of ETP is shown in Fig. 12. At time  $t_2=3.2$  ms, the UFD<sub>1</sub> is fully open,  $T_b$  and  $T_c$  receive turning-on signals.  $T_b$  is turned on due to the forward voltage. The capacitor  $C_{CLP}$  starts to discharge and then is reversely charged. At time  $t_4=4.8$  ms, the capacitor current drops to 0, and  $L_{FCL}$  is completely inserted into the faulty circuit. At time  $t_5=5.3$  ms, SA operates,  $L_{FCL}$  and  $L_{dc1}$  are bypassed. The fault line current is reduced to 0 and the system fault is cleared at time  $t_6=6.7$  ms. The capacitor of ETP begins to absorb the inductor energy after a short period of discharging for 60  $\mu$ s. At time  $t_7=28$  ms, the inductor current drops to 0, CLP returns to the initial state. At time  $t_8=80$  ms, the energy dissipation stage is completed.

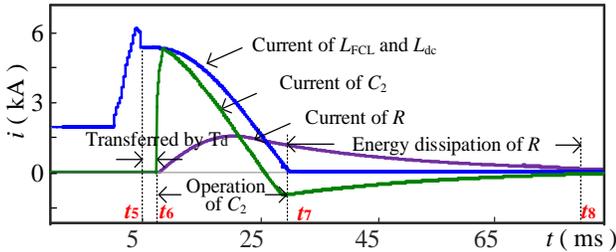


Fig. 12. Internal current of ETP.

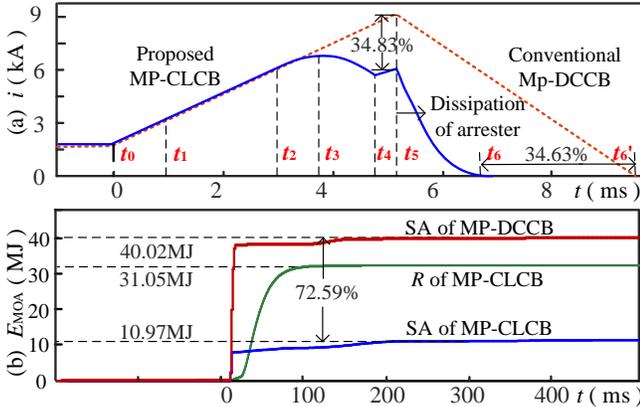


Fig. 13. Comparison of the existing MP-DCCB and MP-CLCB: (a) fault current of line1, (b) energy dissipation of SA and R.

In order to verify the effectiveness of current limiting and energy dissipation of the proposed MP-CLCB, the results are compared with the MP-DCCB proposed in [14]. The comparison of the fault current and the energy dissipation of the SA is shown in Fig. 13.

As seen in Fig. 13(a), compared with the MP-DCCB proposed in [14], the proposed MP-CLCB can reduce the fault current by 34.83% when the SA starts to operate, which can significantly reduce the current stress on each device. The time from when the fault occurs until the faulty line current drops to zero is shortened by 34.63%. As shown in Fig. 13(b), the overall energy dissipation from MP-CLCB's SA and R is similar to the energy dissipated by MP-DCCB's SA. The additional dissipated energy in MP-CLCB is caused by the deployment of the  $L_{FCL}$  which also stores energy. The proposed MP-CLCB reduces 72.59% of the energy to be absorbed by R, which can also reduce the energy consumption requirement of SA. Thanks to the installation of the ETP, the energy dissipation of the inductors is independent from the operation of the grid. The energy dissipation of inductors will also not influence the isolation processes of the faulty line. It is because that the fault isolation process of the breaker is much faster than the period of the energy dissipation. Thus, compared with the complete dissipation in the SA, the fault current on the line decays more quickly, enabling the faulty line to be removed from the system faster. Thus, the system can restore more quickly.

### C. Verification of Reclosing Process

The charging time for  $C_{CLP}$  is about 50 ms and the charging time for  $C_{ETP}$  is about 20 ms. From the fault occurrence to the completion of energy dissipation, it takes 100 ms until the MP-CLCB is able to interrupt next fault current. The de-ionization time of the MP-CLCB is about 200 ms. In the simulation, the reclosing process after clearing the fault is verified as shown in Fig. 14.

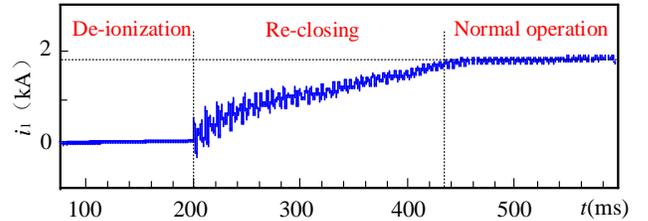


Fig. 14. Line current during the post-fault restoration.

At time  $t=200$  ms, the MBU and  $D_1'$  on the branch are firstly turned on. The voltage on NCP is lowered after about 2.5 ms, at that time UFD<sub>1</sub> starts to close. After about 1 ms, when UFD<sub>1</sub> closes successfully, the  $LCS_1$  is turned on and the MBU is turned off. At  $t=435$  ms, the NCP and Line 1 are restored to the rated operating state. Then, the insulation level of the faulty line is restored. No overcurrent flows through the MBP and the MP-CLCB completes the reclosing process successfully.

## VI. CONCLUSIONS

In this paper, a multi-port current-limiting DC circuit breaker (MP-CLCB) is proposed. The topology, operation process, parameter design and economic analysis are provided. Conclusions are drawn as follows:

By using the main breaker path, the MP-CLCB can reduce the number of DCCBs and FCLs on healthy lines. Compared with the conventional DCCB, the MP-CLCB reduces at least 75.56% of IGBTs at the cost of additional components. In a four-terminal MMC-HVDC system, when the SA starts to operate, the faulty line current is reduced by 34.83% compared with the existing MP-DCCB.

The overall energy dissipation by the SA and  $R$  of the MP-CLCB and by the SA of the MP-DCCB is very similar. However, as the energy dissipation of the SA is assisted by the ETP, the energy dissipation of the SA is reduced by 72.59% compared with the existing MP-DCCB, which significantly reduces the demand for the capacity of SA. The time used to clear the fault is reduced by 34.63% compared to MP-DCCB, which increases the fault current interruption speed. The MP-CLCB needs 80 ms to be ready for the next fault clearance and can reclose within 3.5 ms after the de-ionization process.

Although the proposed MP-CLCB can save numerous IGBTs, it does involve additional components such as capacitors and thyristors which may increase the capital cost. In addition, the added subsystems may influence its reliability in terms of malfunction and wrong signal. Hence, it is worthy of figuring out the trade-off of cost, complexity and reliability without sacrificing the fault protection capability. Moreover, it should be also highlighted that the impact of the triggering delays of different stages and the thyristor recovery behavior on the performance of the topology, although highly desirable to verify its robustness, falls out of the scope of this paper. Last but not least, the internal signal communication of the proposed breaker should be properly designed to avoid the malfunction of power electronics devices and therefore improve its reliability. It would be the future work of the optimal design of the proposed circuit breaker.

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