Improved ADC model of voltage source converters in DC grids

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***Abstract*-- Due to a large number of converters in DC grids, the simulation speed using traditional electromagnetic simulation tools becomes very slow. An ADC (associated discrete circuit) switch model can improve the simulation efficiency greatly by avoiding the modification of system matrix during switching. However, existing ADC switches induce virtual power losses due to simulation errors during switching transients. The mechanism of the virtual power loss is analyzed, and a power loss model is established. An improved ADC switch model is designed by adding compensation sources to mitigate the simulation errors. Theoretical analyses are carried out to prove this improvement. A fast algorithm to obtain the initial values of the compensation sources is proposed by utilizing the complementary operation of IGBTs. The improved ADC switch provides fast simulation speed and high accuracy. The modelling is particularly suitable for investigating long term system dynamics of DC grids with multiple converters and fast converter transients at the same time.**

***Index Terms*—Switches, Modeling, Power losses, Simulation, DC grid**

I. Introduction

High voltage DC grids [1-3] based on voltage source converter (VSC) technologies have been proposed to connect multiple energy sources and AC grids. DC grids can offer high reliability, flexibility and controllability of renewable power transmission and integration [4-6].

Research on DC grids relies on accurate and efficient simulation of DC networks and multiple converters. So far, the commercial off-line power system electromagnetic simulation programs include EMTP-RV, ATP-EMTP, PSCAD-EMTDC, NETOMAC and the Simpower toolbox of MATLAB [7]. The drawback of these off-line electromagnetic simulation programs for DC grids is a slow simulation speed due to a large number of converters. The slow simulation speed would not be acceptable for DC grids with multiple modular multi-level converters (MMC) for tens of seconds of simulation duration in order to investigate system dynamics of both AC and DC networks. It is even more difficult to use these methods for real time simulation.

An averaging model using a mathematic function to represent MMC switching [8-11] can achieve very fast simulation speed. But switching characteristics can not be observed, and abnormal operations such as short-circuit and blocking can not be implemented in this model. In [12], a model has been developed for MMC which expects fast simulation speed by separating the matrix of the converter switches and external networks. However this method causes large simulation errors due to the delay in data exchanging between the converter and the external networks. In addition, the method of separating matrix is not suitable for systems with many converters because more matrix have to be generated which could reduce simulation speed.

The slow simulation is caused by the inefficient processing of switching of converters. Due to the changing of switch states, the conductance matrix of whole network has to be recalculated when the offline simulation programs are used [13].

Currently, there are two approaches to increase simulation speeds: pre-calculation of a conductance matrix [14] and equivalent switch models using the associated discrete circuit (ADC) [15, 16].

The pre-calculation method calculates the inverse of all possible conductance matrixes, which are determined by the states of switches, and stores the results before the simulation. Therefore, the time for calculating inverse matrix during simulation is saved. The drawback is that all the conductance matrixes require large memory capacity. A parallel calculation technology can be used to reduce the size of the matrix by dividing the whole network into several sub-networks [17]. However, some networks are not dividable, when the networks

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are strongly coupled or some components are not suitable for decoupling, such as transmission lines [18, 19].

An ADC switch is represented by an inductor during the ON state and a capacitor during the OFF state. If the "Dommol equivalent conductance" [13] of OFF state are equal to that of ON state, switching actions do not require modifying system conductance matrix. This approach greatly improves the simulation efficiency and it can be easily applied in the existing electromagnetic algorithm.

However, the equivalent capacitors and inductors calculated by the ADC method may not be equal to the parasitic ones of real switches [15, 20]. This discrepancy will induce errors in simulation. Meanwhile, there are large numerical simulation errors of ADC modeling during transient processes [20]. These errors are reflected as switching power losses caused by the numerical integration which do not exist physically. In [21], this kind of switching losses due to the inaccuracy of circuit parameters were observed in simulation but without investigation in depth.

This paper will study the ADC modeling comprehensively. The physical principle of the switching power loss is analyzed. Simple models of switching power losses are established based on the damping of circuits. An improved ADC switch model is proposed in order to remove switching power losses and decrease numerical errors without losing the simulation efficiency of switches.

This method is implemented and tested in a large scale real-time simulation platform ADPSS [22], developed by CEPRI. This platform has been used widely in academic and industrial organizations in China. Simulation is performed to verify the proposed algorithm. This fast and accurate method is particularly suitable for DC grids with multiple voltage sources converters.

II. Review of ADC switch modelling

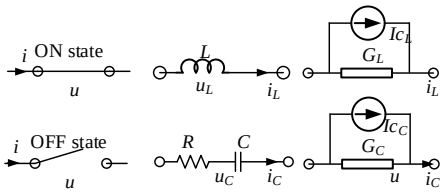


Fig. 1 ADC switch modelling

Models of an ADC switch are illustrated in Fig.1. During the ON state, the switch is represented as an inductor *L*. During the OFF state, the switch is represented as a series connection of a capacitor *C*, and a resistor *R*. The resistor is used to mitigate unexpected oscillation due to the interaction between the capacitor and external inductive circuits. This small resistor has little impact on the switching process of ADC switches [23].

During the ON state, $L\frac{di_L}{dt}=u_L$ which can be represented as (1) by using a backward Euler discretizing method.

$$G_L u_L(n) = i_L(n) + I_{C_L}(n) \tag{1}$$

where $G_L=\Delta T/L$, $I_{C_L}(n)=-i_L(n-1)$, $u_L(n)$ is the switch voltage at the n^{th} simulation time step, $i_L(n)$ is the switch current at the n^{th} time step, and ΔT is the simulation time step. Therefore the inductor branch is modelled as an equivalent conductance G_L in parallel with a companion current source $Ic_L(n)$.

During the OFF state, using the same method, $\frac{d(u_C-i_CR)}{dt}C=i_C$ represented as (2):

$$G_C u_C(n) = i_C(n) + I_{C_C}(n) \tag{2}$$

where $G_C=(R+\Delta T/C)^{-1}$, $I_{C_C}(n)=G_C(u_C(n-1)-i_C(n-1)R$, where $i_C(n)$ and $u_C(n)$ are the switch current and voltage. Therefore the capacitor branch is modelled as an equivalent conductance G_C in parallel with a companion current source $Ic_C(n)$.

The principle of the ADC switch modelling is that the equivalent conductance, G_C and G_L, must be equal in order to avoid the modification of system conductance matrix. Therefore,

$$G=G_L=G_C=\frac{\Delta T}{L}=(R+\frac{\Delta T}{C})^{-1} \tag{3}$$

III. Transient error and switching loss modeling

An ideal switch has zero resistance and zero voltage drop during the ON state and zero leakage current during the OFF state. It should also switch on/off in zero time. However a switching power loss of an ideal switch could be observed due to transient errors of an ADC model.

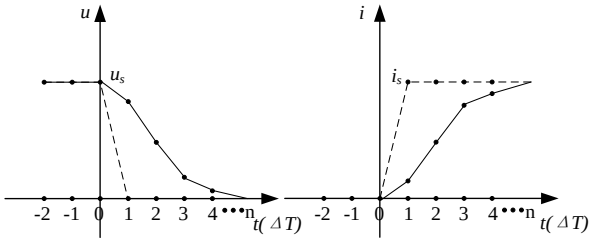


Fig. 2 Switching-on process of ADC switch

Fig. 2 demonstrates the process of switching-on. The dash lines represent the ideal response of a switching-on process, while the solid lines represent an ADC switch.

The switching-on order is sent at the step 0. At this instance, the switching model is modified from the capacitor to the inductor model, as shown in Fig. 1. The initial current of the inductor must be the same as the capacitor which is zero ampere. There is no sudden change of the currents of the inductor and the external circuit.

From the step 1, the ADC switch begins charging, and the current of the equivalent inductor increases gradually before reaching the steady state, and the voltage of the switch decreases to 0 gradually at the same time. The product of the voltage and current of the ADC model is not zero. Correspondingly the energy incurred during this process is not zero either which can be regarded as the energy stored in the inductor.

Similarly, during the switching–off process, a capacitor with zero initial voltage and zero initial energy will replace the inductor of the ADC model. Energy will also be stored in the

capacitor with non-zero voltage after reaching the new steady state (OFF state).

However, the current value of the inductor has to be reset in order for the next switching-on process to replace the capacitor with a zero current in steady state. Due to the similar reason, the capacitor voltage value has to be reset before replacing the inductor during the switching-off. These cause virtual switching losses of an ADC model of an ideal switch.

Fig. 3 is a simple model to analyze the transient response of an ADC switch. An equivalent conductance and paralleled companion current source substitute for the branch of switches. The external circuit is represented as a Norton equivalent circuit, in which I_s is the current source of the external Norton equivalent circuits, and G_{ex} is the equivalent admittance of the external Norton equivalent circuit. *u(n)* is the terminal voltage, and *i(n)* the terminal current in discrete forms.

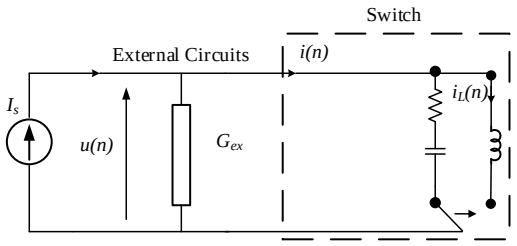


Fig. 3 Small time-step switch modelling

The energy of the inductor and the energy in capacitor are discarded during the switching-off and on process. In every switching circle, the total power loss, E_{loss}, is

$$E_{loss} = E_C + E_L = \frac{1}{2}C(\frac{I_s}{G_{ex}})^2 + \frac{1}{2}I_s{}^2L \tag{4}$$

Because C, L, R and G are not easy to analyze, a factor σ, as given in (5), is proposed to simplify equation.

$$\sigma = \frac{\frac{\Delta T}{C} - R}{\frac{\Delta T}{C} + R} \tag{5}$$

Considering (3), L, C and R can be described as the function of G and σ, as shown in equation (6).

$$\begin{cases} C = \dfrac{2G\Delta T}{1+\sigma} \\ L = \dfrac{\Delta T}{G} \\ R = \dfrac{1-\sigma}{2G} \end{cases} \tag{6}$$

Substituting the expression of the admittance of C and L into (4), the switching power losses can be expressed as

$$E_{loss} = \frac{I_s{}^2}{G_{ex}}(\frac{1}{1+\sigma}(\frac{1}{k}) + \frac{1}{2}k)\Delta T \tag{7}$$

where k is the ratio of external equivalent conductance and the switch equivalent conductance (G_{ex}/G).

Assuming the switch works under the rated condition, when the switch is open, the voltage across the switch is V_{rate}; when the switch is close, the current through switches is I_{rate}. Compared with Fig. 3, the V_{rate} and I_{rate} can be represented by I_s and G_{ex}, as illustrated in equation (8).

$$\begin{cases} V_{rate} = \dfrac{I_s}{G_{ex}} \\ I_{rate} = I_s \end{cases} \tag{8}$$

Therefore the power loss can be rewritten as

$$E_{loss} = V_{rate}I_{rate}(\frac{1}{1+\sigma}(\frac{1}{k}) + \frac{1}{2}k)\Delta T = P_{rate}(\frac{1}{1+\sigma}(\frac{1}{k}) + \frac{1}{2}k)\Delta T \tag{9}$$

It can be seen from (9) that the virtual switching power loss is only related to several factors: P_{rate} (the rated power of the switches), k (the ratio of external equivalent conductance and switching equivalent conductance) and σ (the ratio of resistor in whole branch), not determined by the specific parameters of L or C.

Because the switch model must have efficient damping for the oscillation particularly caused by the existence of the capacitance, the ratio of the resistance in the capacitance branch is normally selected to have the best damping as long as the values of R and C meet the requirements listed in (3). Therefore σ has already been determined using (5). Also, the V_{rate} and I_{rate} of the switches are determined by application, which can not be changed either. Only k can be varied by the user. In addition, k is not related to other factors, so only k needs to be optimized to minimize the virtual switching loss for various applications.

IV. Improved Modelling of ADC Switches

The switching power losses of ADC switches due to discarding the energy stored in the equivalent L and C causes the inaccuracy of simulation. This is the main drawback of the ADC switches. In this section, an improved ADC switch modeling is proposed to compensate the original switching loss. A novel ADC switching algorithm is proposed based on the improved modelling to increase the accuracy of simulation.

A. Unified form of improved modelling of ADC switch

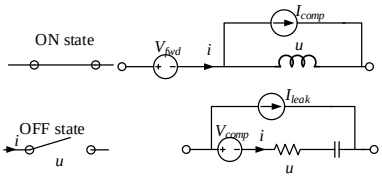


Fig. 4 Improved method of completed unified ADC switches modelling.

Fig. 4 illustrates an improved ADC switch model. Compared with the model shown in Fig. 1, a compensation voltage source, V_{comp}, is added in series with the capacitor branch, and a compensation current source, I_{comp}, is added in parallel with the inductor branch. For a non-ideal switch, a voltage source, V_{fwd} which represents a forward voltage drop, is connected in series for the ON state, while a current source, I_{leak} which represents a leakage current, is connected in parallel for the OFF state, as shown in Fig. 4. Normally, V_{fwd} and I_{leak} are selected to be constant according to switch specifications. V_{fwd} and I_{leak} are zero for an ideal switch. If real switching losses need to be considered in special cases, V_{fwd} can be represented as a function of the switch voltage during ON state,

and I_{leak} can be represented as a function of switch current during OFF state [24-27]. In most cases, modelling of real switching losses has little impact on the dynamic performance of a switch model. The switching loss has not been modeled for a system simulation in most simulation tools, such as RTDS, EMTDC and Simpower [28, 29].

The value of V_{comp} and I_{comp} are set at switching instances. The purpose of the modification of V_{comp} and I_{comp} is to make the state variables of storage elements of the switches to be zero in the steady state.

The voltage $u(\infty)$ or current $i(\infty)$ in the steady state of the switch branch are given in (10),

$$\begin{cases} u(\infty) = \dfrac{I_s - I_{leak}}{G_{ex}} \\ i(\infty) = I_s - V_{fwd} G_{ex} \end{cases} \tag{10}$$

If the compensation sources are set as (11),

$$\begin{cases} V_{comp} = \dfrac{I_s - I_{leak}}{G_{ex}} \\ I_{comp} = I_s - V_{fwd} G_{ex} \end{cases} \tag{11}$$

The steady state values of capacitor voltage and inductor current are calculated as the equation (12),

$$\begin{cases} u_C(\infty) = u(\infty) - V_{comp} = 0 \\ i_L(\infty) = i(\infty) - I_{comp} = 0 \end{cases} \tag{12}$$

Moreover, the initial values of the equivalent capacitor and inductor of the ADC switch at switching instances are 0,

$$\begin{cases} u_C(0) = 0 \\ i_L(0) = 0 \end{cases} \tag{13}$$

In conclusion, because of the initial state and the steady state of the storage elements during the switching process are the same, the energy stored does not change. Also, because the energy of the storage element is zero at the steady state, according to (12), the power losses due to discarding the stored energy become zero.

B. Improvement of transient response based on the improved ADC switching modelling

When the switch is turned on, an equivalent inductor model is used to represent the switch. The improved switch model is used in Fig. 5. The network can be expressed in the equations (14),

$$\begin{cases} i(n) + G_{ex}(u(n) + V_{fwd}) = I_s \\ \mathrm{G}\,u(n) = i_L(n) + Ic_L(n) \\ i_L(n) = i(n) - I_{comp} \end{cases} \tag{14}$$

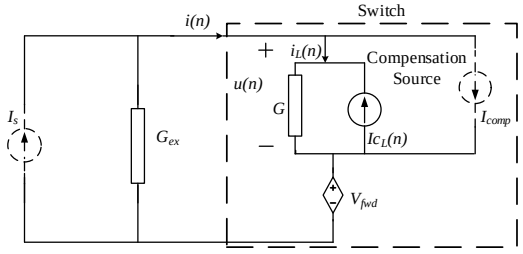


Fig. 5 Improved switch model with compensation sources during ON state

In this equation, $i_L(n)$ represents the current through the equivalent inductor. $Ic_L(n)$ is the companion current source of the equivalent inductor of ADC switch, I_{comp} is the compensation current source.

When the ADC switch is on the ON state, the $Ic_L(n)$ is expressed as (15) according to (1),

$$Ic_L(n) = -i_L(n-1) \tag{15}$$

Substituting the expression of $Ic_L(n)$ to (14), the final equation of network for the improved ADC switch can be rewritten as:

$$\begin{cases} i(n) + G_{ex}(u(n) + V_{fwd}) = I_s \\ \mathrm{G}\,u(n) = i(n) - I_{comp} - (i(n-1) - I_{comp}) \end{cases} \tag{16}$$

According to the initial condition of $i_L(0)$ in equation (13), $i_L(0)=0=i(0)-I_{comp}$. In addition as illustrated in (11), $I_{comp}=I_s-V_{fwd}G_{ex}$. Therefore the equation (17) is obtained.

$$\begin{cases} i(n) + G_{ex}u(n) = I_s - G_{ex}V_{fwd} \\ \mathrm{G}\,u(n) = i(n) - (I_s - G_{ex}V_{fwd}) - (i(n-1) - (I_s - G_{ex}V_{fwd})) \\ i(0) - (I_s - G_{ex}V_{fwd}) = 0 \end{cases} \tag{17}$$

Considering a differential equation with the known initial condition, the solution is unique [30]. Therefore the only solution of these equations is

$$\begin{cases} i(n) = I_s - G_{ex}V_{fwd} \\ u(n) = 0 \end{cases} \tag{18}$$

This means a steady state can be reached without any transient process after the switch is turned on.

Similarly, according to Fig. 5, the equations (19) of the network would be obtained.

$$\begin{cases} i(n) + G_{ex}u(n) = I_s - I_{leak} \\ \mathrm{G}(u(n) - V_{comp}(n)) = i(n) + Ic_C(n) \end{cases} \tag{19}$$

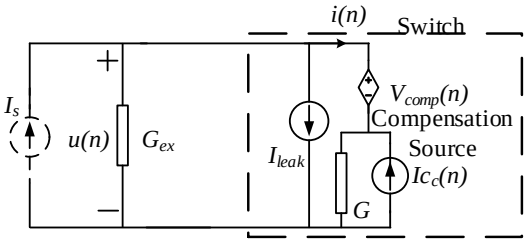


Fig. 6 Improved switch model with compensation source in the OFF state

In this equation, $Ic_C(n)$ is the companion current source of the equivalent capacitor of the ADC switch, V_{comp} is the value of the compensation voltage source.

When the ADC switch is in the OFF state, the $Ic_C(n)$ is illustrated as (2) and V_{comp} is $(I_s-I_{leak})/G_{ex}$ as illustrated in (11) .

Substituting the expression of $Ic_C(n)$ and V_{comp} to (19), the improved ADC switch is expressed as:

$$\begin{cases} i(n) + G_{ex}u(n) = I_s - I_{leak} \\ G(u(n) - \dfrac{I_s - I_{leak}}{G_{ex}}) = i(n) + G(u(n-1) - \dfrac{I_s - I_{leak}}{G_{ex}} - i(\mathrm{n}-1)R) \\ G_{ex}u(0) = I_s - I_{leak} \end{cases} \tag{20}$$

The only solution of these equations is

$$\begin{cases} i(n) = 0 \\ u(n) = \dfrac{I_s - I_{leak}}{G_{ex}} \end{cases} \tag{21}$$

This result shows that although these are dynamic equations, the solution is a constant. The system reaches the

steady state without transient process which is the same as the ideal response. The transient error can be minimized. The power losses can be eliminated by setting proper values of the compensation sources.

V. Algorithm for Obtaining Initial Values of Compensation Sources

By selecting proper values of the compensation sources, transient errors and virtual power losses can be eliminated. However, these values are affected by the external circuits which vary for different topologies and load conditions. A method is designed in this section to determine the values.

Most IGBT based converters use diodes connected in anti-parallel with the IGBTs, such as two-level VSC and half-bridge and H-bridge based modular multilevel converters in DC grids. This paper studies only the converters with all switches operating in pairs.

A two-level three-phase VSC consists of 3 half-bridge converters, and an H-bridge consists of 2 half-bridge converters. Therefore a half-bridge topology is used to illustrate the design algorithm. The equivalent circuit of a half bridge is shown in Fig. 7. Norton equivalent circuits are used to represent the external circuits at the both AC and DC sides. A DC capacitor and an AC inductor are connected to the half-bridge. It is assumed that the DC voltage and AC current are constant during switching transient.

There are four combination states of the half-bridge, as listed in Table.I.

TABLE.I STATE LIST OF TWO LEVEL CONVERTOR

STATE	Upper arm	Lower arm
1	ON	OFF
2	OFF	ON
3	ON	ON
4	OFF	OFF

The states 1 and 2 are in normal operation. The state 3 is a short-circuit, which could damage the converter. The state 4 is in the blocked state of IGBTs with only the diodes in operation. If a dead time is set for switching, both IGBTs are off during the dead time. Therefore the state 4 can be observed during normal operation. However, a typical dead time is about 1μs-2μs, during which the load current continues to flow through the freewheeling diode due to the inductive loads [31]. Commutations always occur between the IGBT of a switch and the freewheeling diode of the other switch in a pair. Therefore a dead time does not affect the switching programming for the states 1 and 2. In this paper, the state 4 considers only the IGBT blocking for a long period when the load current will eventually decay to zero. Three types of state flows are defined as illustrated in Fig.8. Type 1 is between the two normal states; Type 2 is between the normal states and the blocked state; and Type 3 is between the normal states and the short-circuit state.

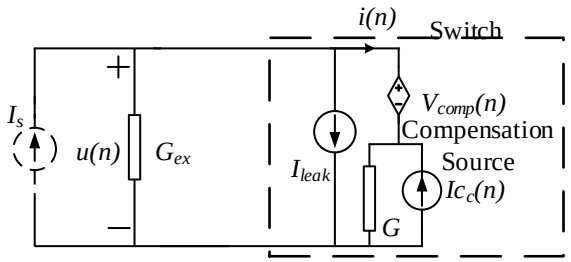


Fig. 7 Topology of half bridge

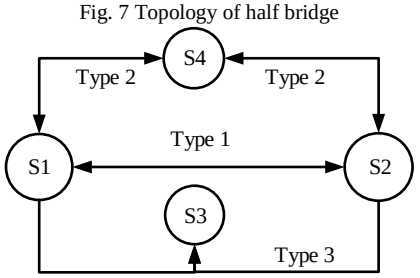


Fig.8 state flow of half bridge

The improved ADC models of the switches are used in Fig.9, in which it is assumed that the upper switch S_1 is in the ON state and the lower switch S_2 is in the OFF state.

***Type 1**: state changes between the states 1 and 2*

Before the switching, S_1 is in the ON state represented as an inductor model and S_2 is in the OFF state represented as a capacitor model. Their currents and voltages are:

$$\begin{cases} u_1(0-)=0 \\ i_1(0-)=i_{ac}+I_{leak2} \\ I_{comp1}(0-)=I_{comp1} \\ Ic_1(0-)=-(i_{ac}+I_{leak2})+I_{comp1} \end{cases} \quad \begin{cases} u_2(0-)=u_{dc}-V_{fwd1} \\ i_2(0-)=0 \\ V_{comp2}(0-)=V_{comp2} \\ Ic_2(0-)=(u_{dc}-V_{fwd1}-V_{comp2})G \end{cases} \tag{22}$$

When the switches change between the states 1 and 2, S_1 is replaced by a capacitor model and S_2 is replaced by an inductor model. The DC voltage u_{dc} does not change instantly because of the DC capacitor, and the AC current i_{ac} does not change instantly either because of the inductor. Therefore, the voltages and currents of the switches become:

$$\begin{cases} u_1(0+)=u_{dc}-V_{fwd2} \\ i_1(0+)=0 \\ V_{comp1}(0+)=u_{dc}-V_{fwd2} \\ Ic_1(0+)=0 \end{cases} \quad \begin{cases} u_2(0+)=0 \\ i_2(0+)=-i_{ac}+I_{leak1} \\ I_{comp2}(0+)=-i_{ac}+I_{leak1} \\ Ic_2(0+)=0 \end{cases} \tag{23}$$

Comparing (22) and (23), the initial value of the compensation voltage source of S_1 can be set as $V_{comp1}(0+)=u_2(0-)+V_{fwd1}-V_{fwd2}$, while the compensation current source of S_2 can be set as $I_{comp2}(0+)=-i_1(0-)+I_{leak2}+I_{leak1}$.

The method is therefore summarized as in (24).

$$\begin{cases} V_{compi}(0+)=u_j(0-)+V_{fwdi}-V_{fwdj} \\ I_{compi}(0+)=-i_j(0-)+I_{leaki}+I_{leakj} \end{cases} \tag{24}$$

where i and j represent the pair of switches operating in complimentary in a half bridge.

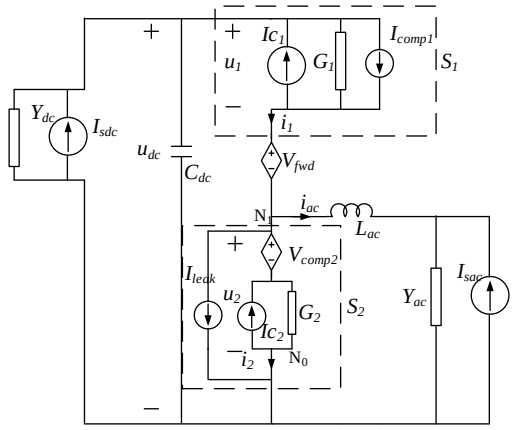


Fig.9 the companion models of half bridge

***Type 2**: state change between the states 1 or 2 and 4.*

These state flows happen in the process of converter blocking and de-blocking.

There are two stages in the converter blocking. First when S_1 is on and S_2 is off, both switches receive the blocking order. The inductive AC load current (assuming positive) commutates from S_1 to the diode of S_2. This process is Type 1.

Then the current through the diode decreases gradually. When the current becomes zero at the time *t*, the converter is blocked. This process is Type 2.

The voltages and currents of the switches at the time *t* are:

$$\begin{cases} u_1(t-) = u_{dc} - V_{fwd2} \\ i_1(t-) = 0 \\ V_{comp1}(t-) = u_{dc} - V_{fwd2} \\ Ic_1(t-) = 0 \end{cases} \quad \begin{cases} u_2(t-) = 0 \\ i_2(t-) = 0 \\ I_{comp2}(t-) = 0 \\ Ic_2(t-) = 0 \end{cases} \tag{25}$$

At this instance, S_2 is switched off suddenly. According to the electrical circuit laws, the voltages and currents of the switches at t=t+ should be:

$$\begin{cases} u_1(t+) = u_{dc} - u_{ac}(t) \\ i_1(t+) = 0 \\ V_{comp1}(t+) = u_{dc} - u_{ac}(t) \\ Ic_1(t+) = 0 \end{cases} \quad \begin{cases} u_2(t+) = u_{ac}(t) \\ i_2(t+) = 0 \\ V_{comp2}(t+) = u_{ac}(t) \\ Ic_2(t+) = 0 \end{cases} \tag{26}$$

In this equation, u_{ac} is the voltage of the external AC circuits, which cannot be determined by the half bridge. In fact, the electromagnetic simulation programs always provide u_{ac} in the previous step, $u_{ac}(t\text{-}\Delta T)$. Therefore $u_{ac}(t\text{-}\Delta T)$ is used to approximate $u_{ac}(t)$. The compensation sources of ADC switches can be set as:

$$\begin{cases} V_{compi}(t+) = u_{ac}(t-\Delta t) \\ V_{compj}(t+) = u_j(t-) - u_{ac}(t-\Delta t) + V_{fwdi} \end{cases} \tag{27}$$

The difference of the initial values at t =t+ are very small, especially when the change rate of i_{ac} is close to 0. Also, this state flow does not always happen in the normal operation. The virtual power losses caused by the errors can be neglected.

In the process of de-blocking from the state 4 to the state 1, the voltages and currents of the blocked switches in the state 4 are illustrated in equation (28):

$$\begin{cases} u_1(0-) = u_{dc} - u_{ac} \\ i_1(0-) = 0 \\ V_{comp1}(0-) = V_{comp1} \\ Ic_1(0-) = (u_{dc} - u_{ac} - V_{comp1})/G \end{cases} \quad \begin{cases} u_2(0-) = u_{ac} \\ i_2(0-) = 0 \\ V_{comp2}(0-) = V_{comp2} \\ Ic_2(0-) = (u_{ac} - V_{comp2})/G \end{cases} \tag{28}$$

where V_{comp1} and V_{comp2} are the values determined by the previous blocking process.

When S_1 is switched on, the voltage, u_{dc}, is only on S_2, and the current through S_1 remains zero. Their voltages and currents of the switches are given in equation (29):

$$\begin{cases} u_1(0+) = 0 \\ i_1(0+) = 0 \\ I_{comp1}(0+) = 0 \\ Ic_1(0+) = 0 \end{cases} \quad \begin{cases} u_2(0+) = u_{dc} - V_{fwd1} \\ i_2(0+) = 0 \\ V_{comp2}(0+) = u_{dc} - V_{fwd1} \\ Ic_2(0+) = 0 \end{cases} \tag{29}$$

The method to set the initial values for the de-blocking can be summarized as:

$$\begin{cases} V_{compi}(0+) = u_j(0-) + u_i(0-) - V_{fwdj} \\ I_{compj}(0+) = 0 \end{cases} \tag{30}$$

***Type 3**: state change from the states 1 or 2 to 3.*

This state change represents a short circuit of the half bridge when both switches are turned on simultaneously by accidents. Before the short circuit, S_1 is ON and S_2 is OFF. Their voltages and currents are given in (23).

When S_2 is turned on suddenly, the inductor model is used for the both switches. The initial short circuit current through the ideal switches is only determined by the DC side circuit, and the voltage and equivalent resistance of the DC capacitor which are hard to determine.

This is a fault condition in operation which does not occur frequently. An approximation is used for the initial values of the compensation current sources as in (31).

$$\begin{cases} I_{compi}(0+) = i_i(0-) + I_{short} \\ I_{compj}(0+) = I_{short} \end{cases} \tag{31}$$

where I_{short} is a typical short circuit current of a half-bridge under certain voltage level and with certain DC capacitance in order for the models reaching real currently quickly. The user of the program can select the value according to their experience or simply set as zero as used in an un-improved ADC model.

VI. CASE STUDY

A multi-terminal HVDC in Fig.10 was used to test the algorithm proposed for VSCs. There are five terminals in the DC grid. The system specifications and parameters are given in TABLE.II. The three-phase voltage source converters have a two-level configuration. An example is shown in the terminal *D*. There have been many control system design for a DC grid [32, 33]. This paper focuses on the switching control only to test the algorithm of improved ADC switches

The simulation and comparison were performed using three simulation platforms, the ADPSS for the unimproved and improved ADC switches, the PSCAD for the ideal switches, and the HVDC grid test platform in Cardiff University, as shown in Fig.11. The ADPSS server is a large scale real-time simulation platform. It consists of CPUs (2×IntelXEON E5-2660 2.2G 8C), memory (4×8G DDR3 1333M) and a hard disk (SAS 300G). The network is used Infiniband with the router of Mellanox MIS5025Q-1SFC QDR. The specifications

and parameters of the 10kW 3-terminal HVDC grid test platform were given in [33].

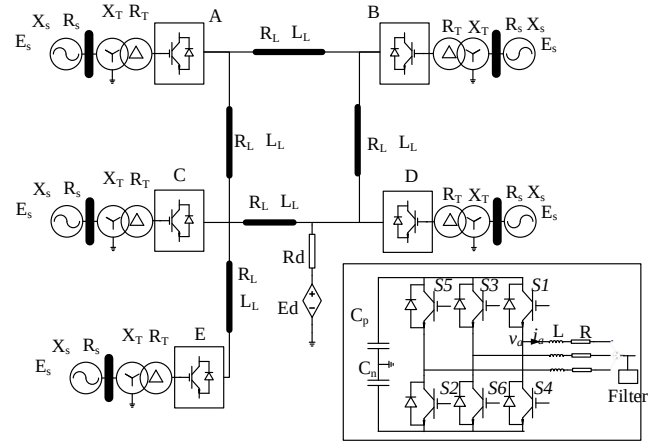


Fig.10 Topology of DC grid with five terminals

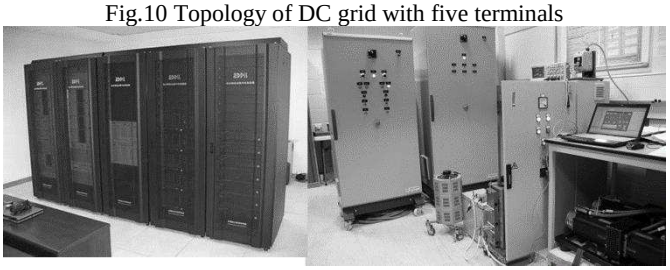


Fig.11 ADPSS platform and HVDC grid test platform [33]

TABLE.II THE PARAMETER OF THE DC GRID

DC sides		AC sides		Switch Parameter	
Cp	100uF	Xs	12.7mH	V_{fwd}	0.01kV
Cn	100uF	Rs	0.1Ω	I_{leak}	0.00001kA
Ed	200kV	X_T	12.7mH		
Rd	10Ω	R_T	2Ω		
fswitching	2000Hz	R	0.01Ω		
R_L	2Ω	L	15.9mH		
L_L	88mH	Pave	70MW		
		Es(L-L)	90kV		

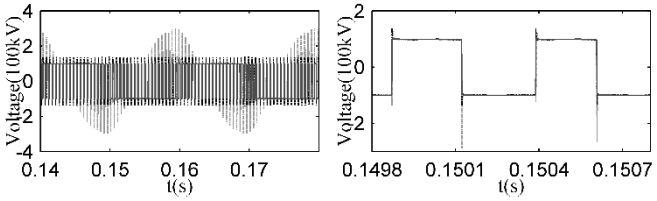
A. Test of accuracy in normal operation

The simulation results of the AC voltage, v_a, and AC current, i_a, of the VSC of the terminal *D* are given in (b)AC Line Current

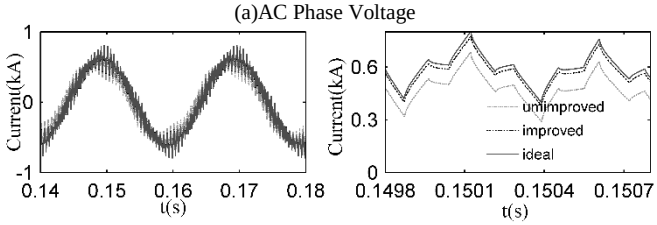
Fig.12. The transient voltage and current of the switch S_1 are given in Fig.13.

At every switching, the unimproved ADC switches experienced a large transient voltage with a peak value up-to 3 times of the DC voltage. Both voltages and currents of the improved switches are consistent to the ideal ones.

Physical experiments were carried out to verify the model. Fig.14 shows the voltage and current of an IGBT during a switching-off process. The DC voltage of the three-phase VSC was set as 180V and the AC load current as 15A. Comparing to the results in Fig.13, the improved ADC model is very close to the experimental results. The transient peak voltage of both ADC model and the experimental result is about 1.3 times of the DC voltage.

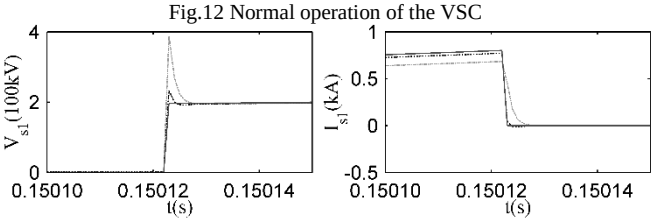


(a)AC Phase Voltage



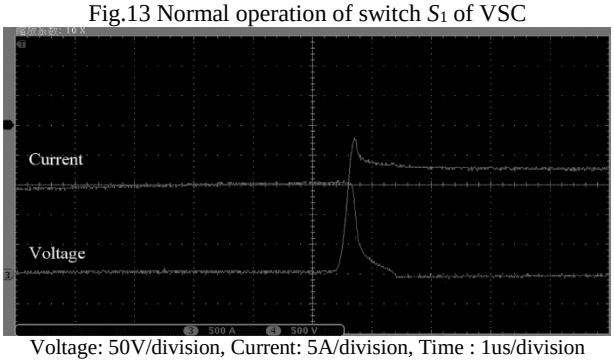
(b)AC Line Current

Fig.12 Normal operation of the VSC



(a)switch voltage (b) switch current

Fig.13 Normal operation of switch S_1 of VSC



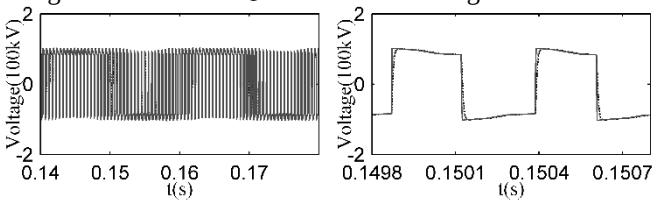
Voltage: 50V/division, Current: 5A/division, Time : 1us/division

Fig.14 Experimental results of a switching-off process of an IGBT in the three-phase VSC

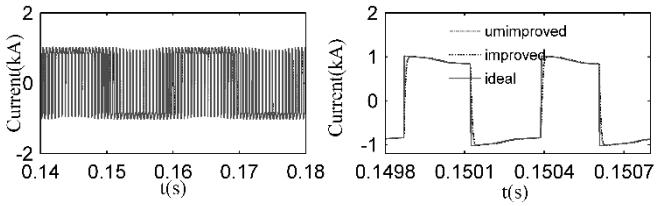
B. Test of accuracy in special cases

Three special operation conditions were used to test the switch models: a converter (e.g. of the terminal D) connects to a purely resistive load only, blocked, and short-circuited suddenly.

Fig.15 shows the results for the resistive load. The transient voltage and current of S_1 are illustrated in Fig.16.



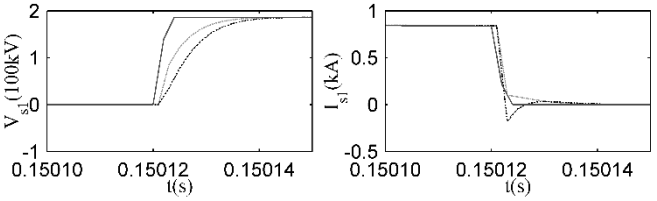
(a)AC Phase Voltage



(b)AC Line Current

Fig.15 VSC connects to a resistor

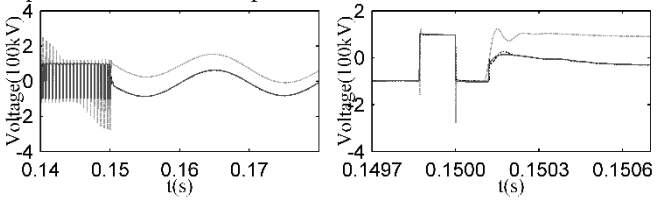
The improved ADC switch does not show advantages in simulation accuracy over the unimproved ADC under the purely resistive load. This is because that the improvement of the ADC switch is based on sufficient large inductance in the AC side. Fortunately most applications of the VSC in HVDC and DC have the inductance from the filters, transformer, lines, and loads.



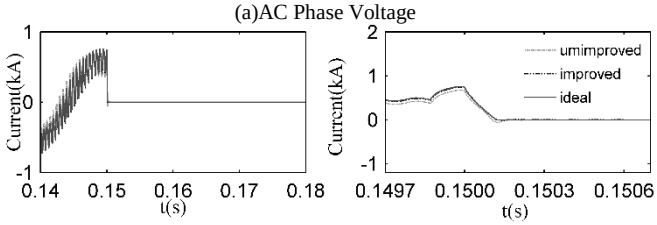
(a)switch voltage (b) switch current

Fig.16 Switch voltage and current under when connecting to a resistor

Fig.17 shows the results for blocking the converter. A blocking signal was sent at 0.15s. All IGBTs are blocked and the current flows through the diodes for about 0.2ms before reaching zero. The improved ADC is much closer to the ideal responses than the unimproved ADC.



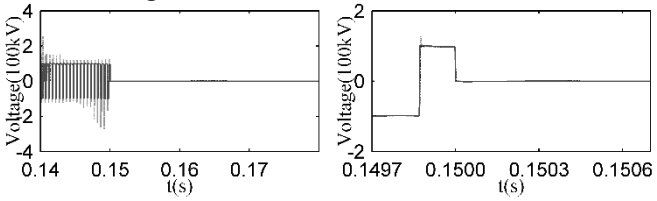
(a)AC Phase Voltage



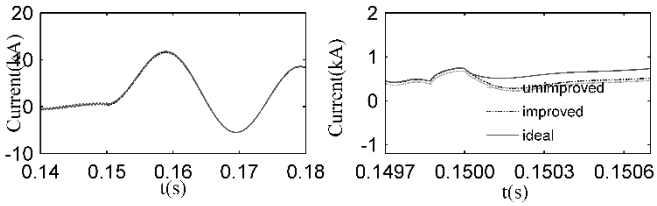
(b)AC Line Current

Fig.17 Blocking responses of the converter

Fig.18 shows the results for the short-circuit of the converter bridge.



(a)AC Phase Voltage



(b)AC Line Current

Fig.18 Short-circuit of converter bridge

In this case, the S_1 and S_4 are both turned on at 0.15s. This results in the short-circuit of the arm and generates large short-circuit current.

From the waveform, the response of either the improved ADC or unimproved ADC switches is not close to the ideal response. The improved ADC has slightly better performance than the unimproved ADC. These errors are acceptable in the simulations for DC grids since the short-circuit does not often occur. The total power energy losses due to the modeling for a short-circuit can be neglected.

C. Test of Power loss

The modeling inaccuracy causes virtual switching power losses of ADC switches. In order to verify the relationship between the power loss and the conductance ratio *k* (the ratio of external circuit conductance to the ADC switches in equation (7)), different system parameters, L, R and C, are used for a converter to achieve different losses. The results are listed in TABEL.III.

Although the *L*, *R*, *C* are different, as long as the ratio, *k*, is the same, the power loss is the same. The power losses are only determined by the *k*.

TABEL.III THE PARAMETER OF ADC SWITCHES FOR SWITCHING POWER LOSS TEST

L(mH)	R(mΩ)	C(nF)	V_{rate}	I_{rate}	k	Loss
0.94	0.093	0.32	200kV	0.8kA	9.0533	13.4%
0.21	0.42	1.45	200kV	0.8kA	2.2633	6.89%
0.83	0.11	0.36	400kV	0.4kA	2.2633	6.89%

Proper selection of the *k* helps to minimize the virtual power loss. Fig. 19 shows the virtual power losses using different integration methods when *k* varies from the 0.5 to 9.5. The solid line, *ADC-esti*, represents the estimated results of an unimproved ADC switches calculated according to the equation (9), while the dash line represents the simulation result the unimproved ADC switch.

For a comparison, the result of the improved ADC switch, and the ideal switch are also shown in Fig. 19. The power loss for an ideal switch and the improved ADC model of an ideal switch are both close to zero.

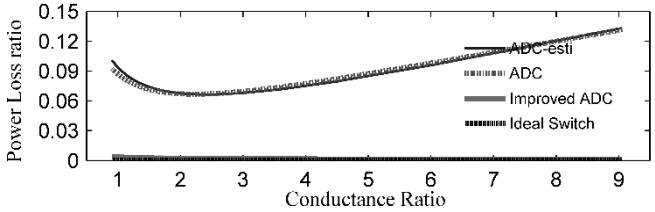


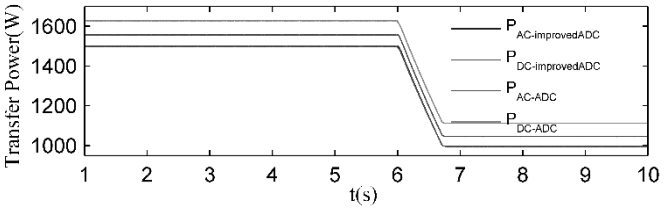
Fig. 19 Power losses of different switch model

To verify the improved ADC modeling for a real switch with power losses, the power losses of a three-phase two-level

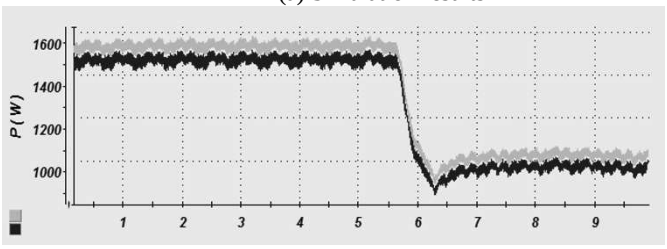
VSC converter using an ADC model, the improved ADC model and the HVDC test rig were obtained, as shown in Fig.20. In the experiment, about 1500W real power is delivered to the AC side, and the DC side power is 1560W as shown in Fig.20(b). The power loss is about 60W. At about 6 second, the AC real power is ramped down to 1000W, the corresponding DC side power is 1050W, and the power loss is about 50W.

When the improved ADC model is used, as shown in Fig.20(a), the simulation results of the AC side power, $P_{AC\text{-}improved\text{-}ADC.}$, the DC side power, $P_{DC\text{-}improved\text{-}ADC,}$ and power loss ($=P_{DC\text{-}improved\text{-}ADC}-P_{AC\text{-}improved\text{-}ADC}$) are almost the same as the experimental results.

When an unimproved ADC model is used, the AC side power, $P_{AC\text{-}ADC}$, is ramped down from 1500W to 1000W. The DC side power, $P_{DC\text{-}ADC}$, are 1628W and 1112W respectively. So the power loss are about 128W and 112W, which are 68W and 62W higher than the actual power losses. This is due to the virtual switching power loss of unimproved ADC models.



(a) Simulation results



(b) experimental results

Fig. 20 Power losses of a three-phase VSC converter

D. Test of simulation speed

Tests were made to compare the simulation speeds of the improved ADC model in ADPSS and the ideal switch in PSCAD using a typical PC. In order to evaluate the simulation speed of ADC switches, ADPSS and PSCAD programs are run using the same laptop.

Simulation times for different network scales with different numbers of VSCs are given in TABLE.IV. In these tests, the simulation duration is 2 seconds and the simulation time step is 1μs.

TABLE.IV SIMULATION TIME FOR DIFFERENT SWITCHES MODELING

Conv num.	Node	Branch	Switch	Simulation duration	Improved ADC	Ideal switch
1	28	58	12	2s	37s	69s
3	78	164	36	2s	75s	214s
5	128	270	60	2s	125s	489s

The simulation time for the improved ADC switches is much less than that for ideal switches. As the number of VSCs increase, the advantage of the ADC switches is more significant. Hence the ADC switches are extremely suitable for a large scale network, for example DC grids, FACTS and other multiple VSCs application.

When this case study is preformed on the ADPSS Sever, as shown in Fig. 11, the results of the simulation times are given in Table.V.

TABLE.V SIMULATION TIME FOR DIFFERENT SWITCHES MODELING IN ADPSS INTEL SERVER

Conv num.	Simulation duration	Improved ADC		Ideal switch	
		normal	parallel	normal	parallel
1	2s	18.72s	18.72	35.87s	35.87
3	2s	45.39s	20.45	83.67	38.76
5	2s	67.8s	21.65	238.6s	40.12

Nevertheless, the simulation has not yet achieved real-time. FPGA may be a solution for the real-time simulation of DC grids.

E. Test of multi-modular converter (MMC)

The improved ADC model can not only be used for two-level converters but also for various types of multi-level converter including MMC, Neutral-Point-Clamped (NPC) converters and flying capacitor converters since all the IGBTs are operating in pairs. MMC will be the major converters for future DC grids. Therefore, as an example, a three-phase MMC, as shown in Fig.21, was built using both the improved ADC and ideal model in PSCAD.

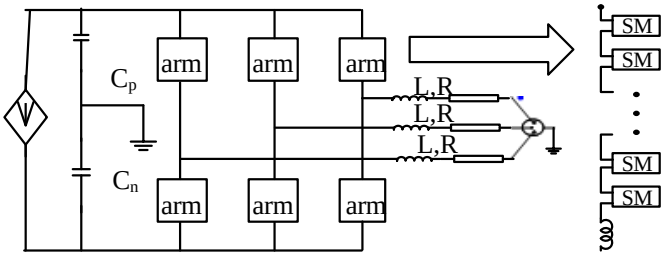


Fig.21 The topology of the MMC

The AC side of MMC is directly connected to an inductive load. Each arm contains 15 half-bridge based sub-modules. The voltage of every sub-module is assumed to be balanced. The simulation results of the AC voltage and the DC voltage are shown in Fig.22.

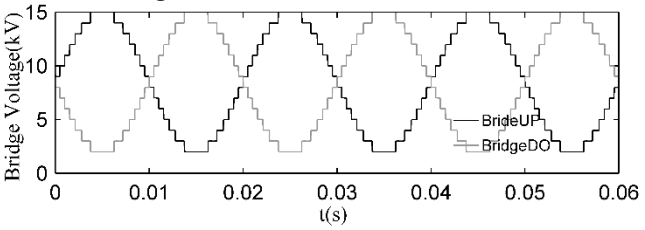


Fig.22 Result of the case of MMC

The simulation time for one MMC is shown in TABLE.VI. For a comparison, simulation time for one 3-phase 2-level VSC is also given. Since there are much more switches in MMC than in a 2-level VSC, it takes quite long time to simulate the MMC. However the time consumption has been significantly reduced from the PSCAD models. It has become realistic to simulate a DC grid with multiple MMC for a longer period to test the dynamic performance of transmission

networks, and with sufficient accuracy of every IGBT switch.

TABLE.VI SIMULATION TIME FOR DIFFERENT VSC TOPOLOGIES

Conv num.	Node	Branch	Switch	Duration	Improved ADC	Ideal switch
1_{MMC}	276	398	180	0.3s	123s	6765s
$1_{2\text{-level VSC}}$	28	58	12	0.3s	7s	10s

VII. CONCLUSION

This paper analyzes in-depth the ADC switch modeling for simulation. The ADC switches can greatly improve the simulation efficiency by avoiding the modification of system matrix during switching. However, resetting the initial values of each switching causes the simulation errors which are reflected as virtual switching power losses even for an ideal switch.

A mathematical model of the virtual power loss has been established. This model demonstrates the relationship of power loss and the parameter of ADC switches, and shows that the modification of parameter of ADC switches only can not eliminate the virtual switching power loss.

An improved ADC model is proposed by adding compensation voltage and current sources to mitigate the simulation errors. A key contribution in this study is to find method to determine the initial value of the compensation source of the improved ADC switches by using the complementary operation of IGBT pairs.

Simulations have been performed for VSC under normal operation, short-circuit of converter bridges, converter blocking and modular multi-level configuration to test the proposed model. Simulation results prove that the improved ADC model is fast in simulation, accurate in switching process, and suitable for large system with multiple converters.

It should be noted that although only the modeling of an ideal switch is investigated in this study, the models of practical switches with real power losses can be easily achieved, e.g. by adding equivalent resistance or voltage drops, based on the ideal model.

The proposed model is particularly suitable for multi-terminal HVDC grids to investigate both converter transient in micro-second range and system dynamics in tens of seconds range. It is also suitable for other systems with multiple FACTS and HVDC links.

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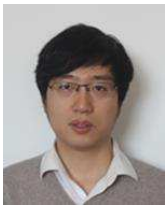

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