Wideband Active Envelope Load-Pull for Robust Power Amplifier and Transistor Characterisation

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By

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ABSTRACT

The advent of fourth generation (4G) wireless communication with available modulation bandwidth ranging from 1 MHz to 20 MHz is starting to emerge. The type of modulation techniques being employed means that the power amplifiers that support the standards need to have high degree of linearity. By nature, however, all power amplifiers are non-linear. Load-pull measurement system provides an indispensable non-linear tool for the characterization of power amplifier and transistor for linearity enhancement. Conventional passive or active load-pull systems have a problem providing a constant impedance that gets worse as the modulation frequency is increased beyond a few MHz. Furthermore, in order to provide robust non-linear measurements, load-pull systems need to provide bandwidth at least five times the modulation bandwidth in order to include the fifth-order inter-modulation (IMD5) terms. This thesis presents, for the first time, a delay compensated non-iterative active envelope load-pull architecture that can provide constant impedance for bandwidths up to 20 MHz with at least 37 dB dynamic range. In order to verify the potential advantages of the new load-pull system, power amplifier linearity investigations and transistor characterisations have been performed using the load-pull integrated with multi-tone non-linear measurement system. It provides a superior load-pull measurement that presents constant load impedances across multi-tone in non-iterative fashion. It also has the ability to directly control all in-band impedances without resorting to out-of-band control. Engineered variations imposed on the in-band impedances offer further insight on power amplifier and transistor behaviours under wideband multi-tone stimulus.

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LIST OF PUBLICATIONS

Conference Paper:

1. Hashim S.J., Hashmi M.S., Jonathan Benedikt J. and Tasker P.J., "*FPGA-Based Digital RF Control for Active Envelope Load-Pull System*", IET Postgraduate Workshop on Microelectronics and Embedded Systems, Birmingham, October 2006

2. Hashim S.J., Hashmi M.S.,Williams T., Woodington S., Benedikt J. and Tasker P.J., "*Active Envelope Load-pull for Wideband Multi-tone Stimulus Incorporating Delay Compensation*", In Proc. Of 38th European Microwave Conference, Amsterdam, October 2008, Pages: 317-320

3. Hashim S.J., Benedikt J. and Tasker P.J., "*Investigation of RF In-Band Impedance Variations on Power Transistor Dynamic Transfer Characteristics*", Asia Pacific Symposium of Applied Electromagnetics and Mechanics, Kuala Lumpur, Jul 2010

4. Hashim S.J., Hashmi M.S, Benedikt J. and Tasker P.J., "*Effect of Impedance Variation around the Fundamentals on PA Distortions Characteristics under Wideband Multi-Tone Stimulus*", Accepted in IEEE Asia Pacific Conference on Circuit and Systems, Kuala Lumpur, Dec 2010

Design paper:

5. Hashmi M.S, Hashim S.J, Woodington, S, Williams T., Benedikt J. and Tasker P.J., "*Active Envelope Load-pull Solution Addressing the RF Device Characterization Problem*", IEEE MTT-11 Design on Originality and Creativity, Atlanta, Jun 2008, 3rd Place, Pages: 6-7

LIST OF ACRONYM

ADC	Analogue to Digital Converter
ALC	Automatic Level Control
ALUT	Adaptive Look-Up Table
AM	Amplitude Modulation
AM-AM	Amplitude Modulation - Amplitude Modulation
AM-PM	Amplitude Modulation - Phase Modulation
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Signal Processor
AWG	Arbitrary Waveform Generator
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CODEC	Coder/Decoder
CPU	Central Processing Unit
CW	Continuous Wave
DAC	Digital to Analogue Converter
dB	Decibel
dBc	Decibel Relative to Carrier
dBm	Decibel Reference to 1 Milliwatt
DC	Direct Current
DSO	Digital Sampling Oscilloscope
DSP	Digital signal Processing
DUT	Device Under Test
EDGE	Enhanced Data rates for GSM Evolution
ESG	Electronic Signal Generator
F1	Lower Fundamental
F2	Upper Fundamental
FDMA	Frequency Division Multiple Access
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array

GaN	Gallium Nitride
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HDL	hardware Description Language
HFET	Heterostructure Field Effect Transistor
ISMCE	In-System Memory Content Editor
IFFT	Inverse Fast Fourier Transform
IP	Intellectual Property
I/Q	In-Phase/Quadrature
IMD3	Third Order Inter-modulation Distortion
IMD5	Fifth Order Inter-modulation Distortion
IMD7	Seventh Order Inter-modulation Distortion
IMD9	Ninth Order Inter-modulation Distortion
ISMCE	In-System Memory Content Editor
JTAG	Joint Test Action Group
LTE	Long Term Evolution
LO	Local Oscillator
LUT	Look-Up Table
MAC	Multiply Accumulate
MPU	Micro Processor Unit
MSPS	Mega Sample Per Second
OFDMA	Orthogonal Frequency Domain Multiple Access
PA	Power Amplifier
PAE	Power Added Efficiency
PLL	Phase Lock-Loop
PC	Personal Computer
PSG	Programmable Signal Generator
RAM	Random Access memory
RF	Radio Frequency
SMA	Sub Miniature Version A
STP	Signal Tap Processing

TDMA	Time Division Multiple Access
VHDL	VHSIC (Very High Speed Integrated Circuits) HDL
WIMAX	Worldwide Interoperability of Microwave Access
WCDMA	Wideband Code Division Multiple Access
VLSI	Very Large Scale Integration
VNA	Vector Network Analyser

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CHAPTER 1

INTRODUCTION

1.1 Power Amplifier for Wireless Communication System

Wireless communication has experienced radical transformation in the last few years. Wireless communication is not only being used for transporting voice but also increasing networking data. People nowadays demanding personal computer (PC) functionality on their phone when they are on the move, therefore, the phone has becoming more like a PC in terms of functionality. This new breed of mobile phone is called *smartphone*. Majority of new released mobile phones are in the smartphone category for example Apple iPhone, Google Nexus One and Palm Pre.

The smartphone phenomenon has caught the power amplifier industry by surprised. It is not very long ago that most mobile phone wireless standards used constant envelope signal but now almost all smartphone uses variable envelope signal with variation in both phase and amplitude for better spectral efficiency. Unlike constant envelope signal, the variable envelope signal requires high degree of linearity [1]. Smartphone features multi-tasking capability similar to the PC. This multi-tasking activity drains more battery than the single-tasking activity. The RF transmission using power amplifier is a well known major power user in any mobile phone. The new trend is to increase the power efficiency to lengthen mobile usage between recharging.

The fourth generation (4G) mobile wireless standard LTE was designed from the start not to put too stringent a linearity requirement on the system by adopting single carrier instead of multiple carrier approach for uplink transmission [2]. Mobile WIMAX wireless standard took a different route, instead of using single carrier for up-link, it adopted multi carrier approach for both uplink and down link. Regardless of the de facto wireless standard that eventually will be popular in the future, the main task for power amplifier designer is to design with linearity in mind. The key to developing linear circuits for LTE or Mobile WIMAX based systems is to first characterise the nonlinear behaviour of the core active device. Devices that do not have a linear input/output relationship are going to be a major contributor to information interference and the reduction in effective bandwidth [3].

1.2 Research Motivations

There are two main drivers for this thesis project. Firstly is the development trend of modern communication standard that are always increasing in complexity. Second driver is the three important components in power amplifier design namely measurement, simulation and modelling. There is a need for measurement and load-pull hardware with similar capability as the simulation and modelling.

1.2.1 Modern Wireless Communication Standard Trends

Over the years the consumer market for mobile phone has increased rapidly around the world. The ownership is roughly from one per household to one for every member of the family in the developed countries. Catering for multitude of consumers of different age

groups, different background and genders has push generic mobile functionality, as has been mentioned before, to be more like a PC. This is reflected by the move toward more complicated standards as shown in Table 1.1. The obvious trend is for more bandwidth and variable envelope signal. These two features ultimately enable support for wide bandwidth application such as video streaming to the mobile phone.

Table 1.1: Modern Mobile Wireless Communication Standard Trends and Comparison

	GSM	GPRS	EDGE	WCDMA	LTE	WIMAX
Generation	2G	2.5G	2.5G	3G	4G	4G
Multiple Access	TDMA	TDMA	TDMA	CDMA	OFDMA	OFDMA
Duplexing	Frequency Division				Frequency and Time	Frequency and Time
Modulation	GMSK	GMSK	8-PSK	QPSK	QPSK, QAM	QPSK, QAM
Signal envelope	Constant	Constant	Variable	Variable	Variable	Variable
Power control range	Small (about 25 dB)			Wide (more than 74 dB)		
Uplink Data Rate (kbps)	9.6 – 14.4	171.2	384	5760	35000	144000
Downlink Data Rate (kbps)	9.6 – 14.4	171.2	384	14400	35000	144000
Channel BW (MHz)	0.2	0.2	0.2	5	20	20
Channel BW up to IMD5 (MHz)	**1**	**1**	**1**	**25**	**100**	**100**

Variable amplitude and phase envelope signal is used for better spectral efficiency. This in turn requires better linearity measurement for the power amplifier. Higher bandwidth requirement for communication means demands for much higher bandwidth for measurement system with at least five times the modulation bandwidth in order to include the fifth order inter-modulation distortions (IMD5) components. The emerging 4^{th} generation networks can have up to 20 MHz bandwidth. This bandwidth translates to 100 MHz for linearity measurement.

1.2.2 Measurement, Simulation and Modelling for Power Amplifier

Measurement, simulation and modelling are very important for successful power amplifier design [4]. Power transistor vendors provide circuit designers with technical information on their devices in data sheets for helping with power amplifier design. However, the description of device behaviour in these documents is valid only for limited electrical and thermal conditions. In general, I-V characteristic and S-parameter sets of a few bias conditions are provided for the computer-aided design circuit. However, these data sets are only useful for design of small signal applications, where the range of the active load line does not cover a large area in the I-V characteristic and the operating point is identical or close to bias-points, for which the S-parameter sets are available.

In some cases, transistor vendors also offer models for their devices. But there also, the validity of the models is limited since the model parameters are extracted from measurements under specific conditions which mostly deviate from the actual operating conditions [5]. Thus, for large signal power applications, it is necessary to measure and characterise the transistor under realistic operating conditions and perform the model

parameter extraction from these measurement data. With this approach, the extracted models used in a computer aided design (CAD) tool should be capable of describing accurately the device behaviour under realistic operating conditions.

According to Table 1.2 the RF simulation and modelling community has come up with useful techniques for supporting the design of a power amplifier. The measurement community, however, is trailing behind in the area of measurement equivalent to the envelope domain simulation. The measurement of modern power amplifiers involving wideband modulated stimulus is difficult and slow. The focus of this thesis is to partly fill the gap in the measurement world related to the envelope domain capability.

Table 1.2: Measurement, simulation and modelling for power amplifier (PA) characterization

Measurement	**Simulation**	**Modelling**
Vector Network Analyzer (VNA)	Linear frequency domain technique	Small signal RF; S-parameters
Non-linear VNA with harmonic load-pull	Harmonic balance technique	Large signal RF; time domain waveforms
?	Envelope technique	Modulated large signal RF; envelope domain waveforms

Measurement hardware, for example signal generator, have managed to keep up with the requirement with modulation bandwidth in excess of 100 MHz but the load-pull hardware does not. Hence there is a need for load-pull hardware solution that is capable of providing load emulation impedance control for wide bandwidth stimuli [6,7].

1.3 Load-Pull Taxonomy

Due to multiple number of load-pull techniques available it is helpful to have some kind of load-pull classification or taxonomy in order to understand the research domain. Figure 1.1 provides rather comprehensive load-pull taxonomy.

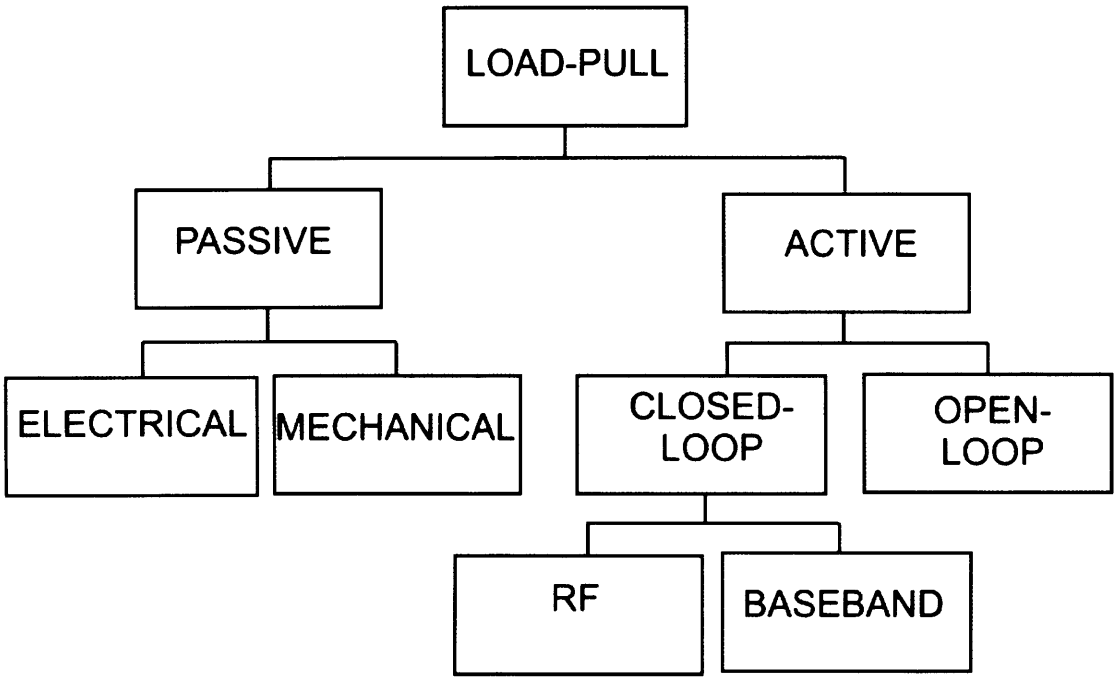

Figure 1.1: Load-pull taxonomy

There are two facets of load-pull measurement in relation to power amplifier design, complexity and bandwidth as shown in Figure 1.2. The complexity and bandwidth are driven mostly by the modern wireless standard trends. Active envelope load-pull tries to fill the void between CW and modulated measurement as indicated by the dotted line inside Figure 1.2. This involves supporting an increased stimulus complexity and greater bandwidth. This new functionality will allow for characterisation of the power amplifier and transistor using more realistic stimulus in a constant impedance environment.

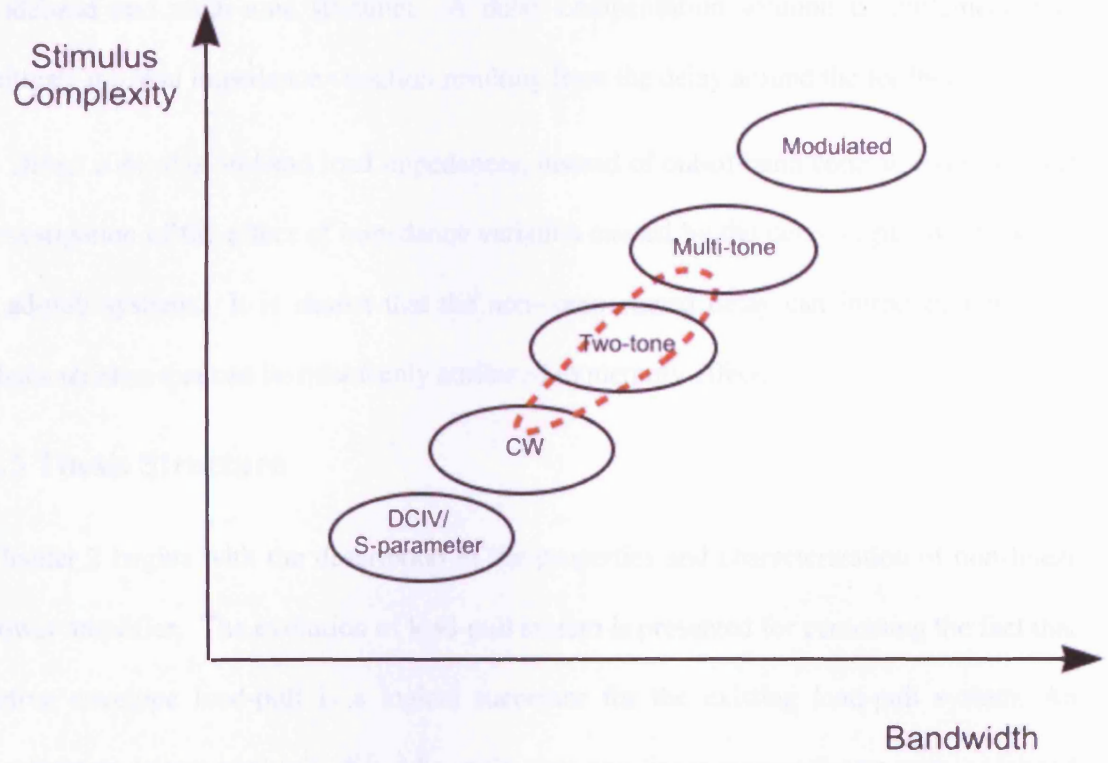

Figure 1.2 :Measurement stimulus complexity against bandwidth for characterisation of power amplifier and transistor

1.4 Thesis Contributions

The purpose of the thesis mainly is to provide a viable load-pull solution that can handle the increasing complexity and bandwidth of the stimulus used in wideband power amplifier characterisation. The implemented envelope load-pull architecture supports fully synchronised operation between the reflected Γ and the output of the DUT. The architecture also supports adaptive operation suitable for dynamic stimulus and biasing condition as normally experienced by modern wireless power amplifier.

A digital controller for Active Envelope Load Pull was developed that can support wideband and multi-tone stimulus. A delay compensation solution is implemented to mitigate the load impedance variation resulting from the delay around the feedback loop.

Direct control of in-band load impedances, instead of out-of-band control, enables novel investigation of the effect of impedance variation caused by the delay in passive or active load-pull systems. It is shown that the non-compensated delay can introduce non-ideal characteristics that can be mistakenly attributed to memory effect.

1.5 Thesis Structure

Chapter 2 begins with the description of the properties and characterization of non-linear power amplifier. The evolution of load-pull system is presented for cementing the fact that active envelope load-pull is a logical successor for the existing load-pull system. An explanation is provided to justify why multi-tone non-linear measurements with wideband active envelope load-pull is an ideal solution for modern power amplifier design and characterisation. Overview of the FPGA platform is presented for understanding how wideband capability of digital controller is feasible.

Chapter 3 focuses on the development of the FPGA based digital controller. FPGA fundamentals and development techniques are presented for basic understanding of prototyping using FPGA. Actual design and implementation of the digital controller using Quartus software is given, with each of the functional blocks being described and explained in the context of active envelope load-pull prototyping activity. The chapter ends with the

prototyping of the digital controller using the FPGA development board. The bandwidth related issues are explained and the implemented solutions are presented.

Chapter 4 provides verification of the developed digital controller. The digital controller is integrated into multi-tone measurement system. The delay around the feedback loop is successfully compensated using the memory based delay implemented inside the digital controller. Then, the adaptive functionality of the load-pull system is verified using phase and amplitude swept stimulus. The active envelope load-pull capabilities including dynamic range and bandwidth were investigated. Ability to provide constant load emulation across several modulation frequency is also demonstrated.

Chapter 5 demonstrates the application of active envelope load-pull in characterising both power amplifiers and transistors. Linearity contours of a packaged power amplifier are presented with minimum corruption due to the comprehensive wideband load impedance emulation including the inter-modulation distortions. The effect of the RF in-band impedance on power transistor dynamic characteristics is investigated.

Chapter 6 concludes the whole thesis by briefly summarising the main points of the thesis and pointing to several problems that should be explored further in order to make the active envelope load-pull measurement system more effective for power amplifier design and characterisation.

1.6 References

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CHAPTER 2

LOAD-PULL SYSTEM FOR NON-LINEAR RF POWER TRANSISTOR CHARACTERISATION

2.1 Properties of Non-linear RF Power Amplifiers

Power amplifiers are non-linear circuits whose main goal is the amplification of a large signal at a given frequency, or rather, in a given frequency band [1]. Using the law of conversation of energy that "energy is neither created nor distroyed", power amplifiers get the extra energy for its output by utilising the energy from its bias network. A simplified diagram of power amplifier's power budget is given in Figure 2.1.

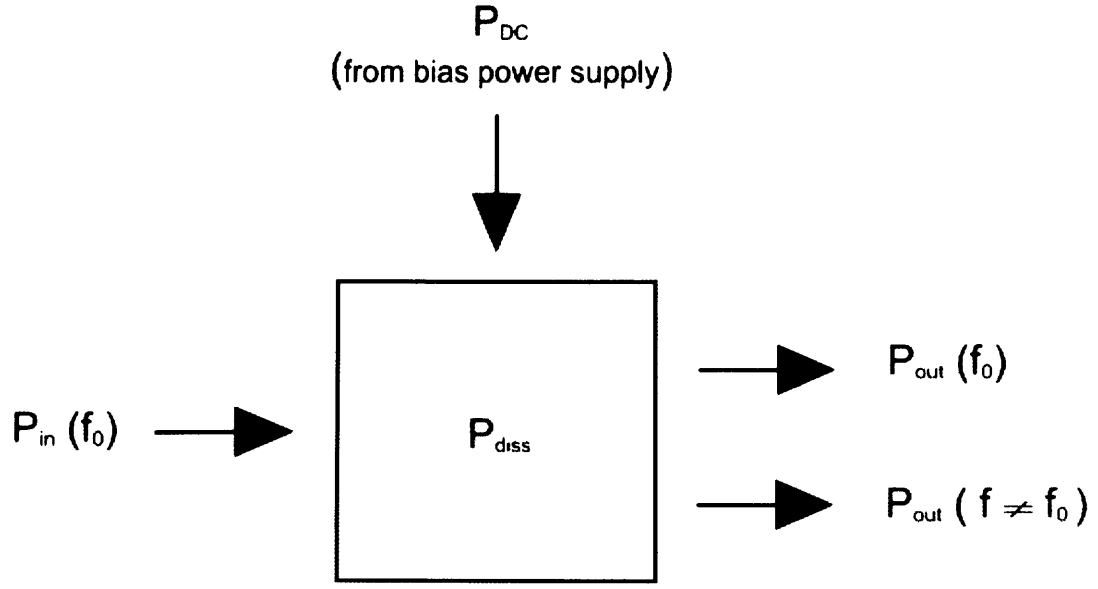

Figure 2.1: Power budget in a power amplifier [1]

The frequency f_0 is frequency band of interest. The power balance is given by

$$P_{DC} + P_{in}(f_0) = P_{out}(f_0) + P_{out}(f \neq f_0) + P_{diss} \quad (2.1)$$

The output power outside the frequency band of interest, $P_{out}(f \neq f_0)$, is considered distortion and falls either under harmonic distortion (HD) or inter-modulation distortions (IMD). The most troublesome is the IMDs because it can interfere with adjacent signal in different communication bands and due to its proximity with the main signal, it may not be excluded by a band-pass filter. The linearisation of the power amplifier by minimising IMD is one of the important research activities in power amplifier design and characterisation. Figure 2.2 displays power amplifier non-linear response for two-tone and CDMA around fundamentals.

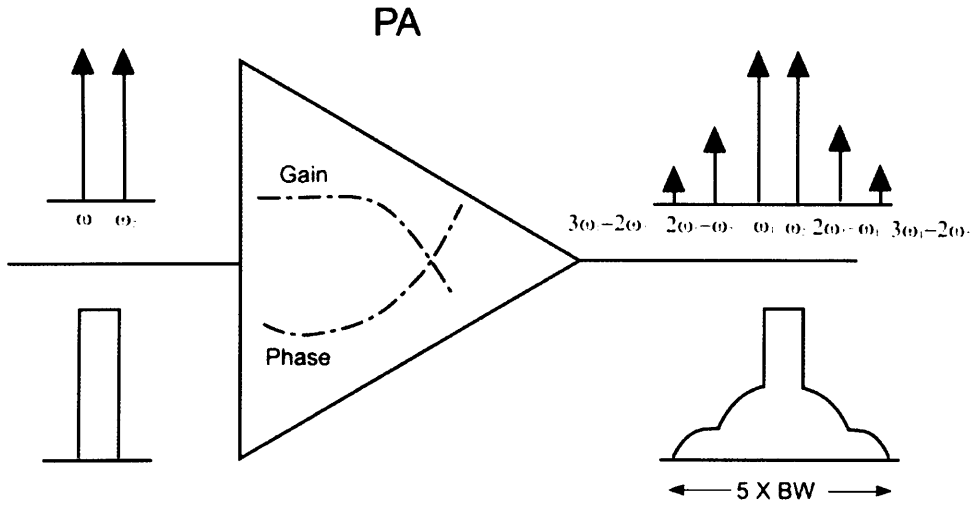

Figure 2.2: Power amplifier non-linear output for two-tone and CDMA signals around fundamentals [2]

A power amplifier that exhibits these distortions is called non-linear power amplifier. All RF power amplifiers by definition are non-linear but normally they are operated at

back-off power levels (linear operating region) with minimum distortions. The penalty of this approach is that the power amplifier will operate at a lower efficiency than theoretically possible. For example a small 3 dB back-off will halve the efficiency of ideal class A power amplifier from 50% to 25% [3]. Efficiency is another important field of research in power amplifier design and characterisation. Figure 2.3 shows an example of output power, power gain and power-added efficiency (PAE) for RF power amplifier including the 1 dB compression point.

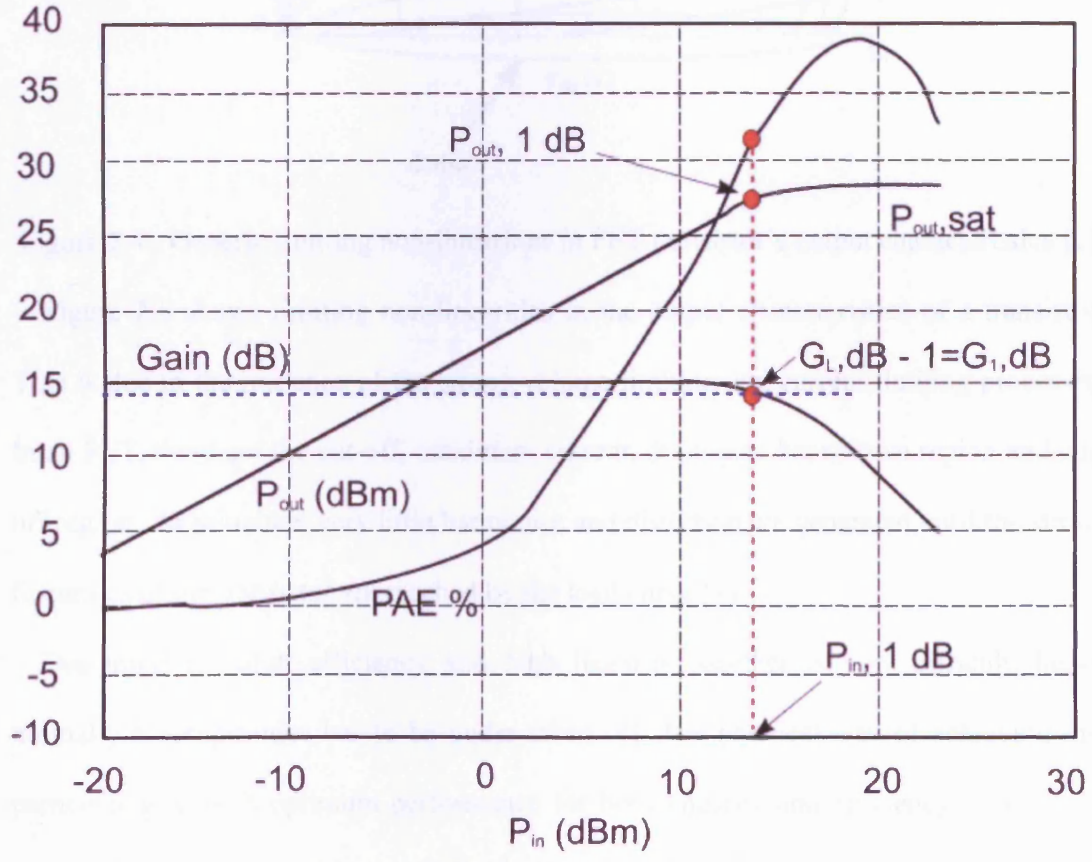

Figure 2.3: Generic output power, power gain and PAE as a function of input power [1]

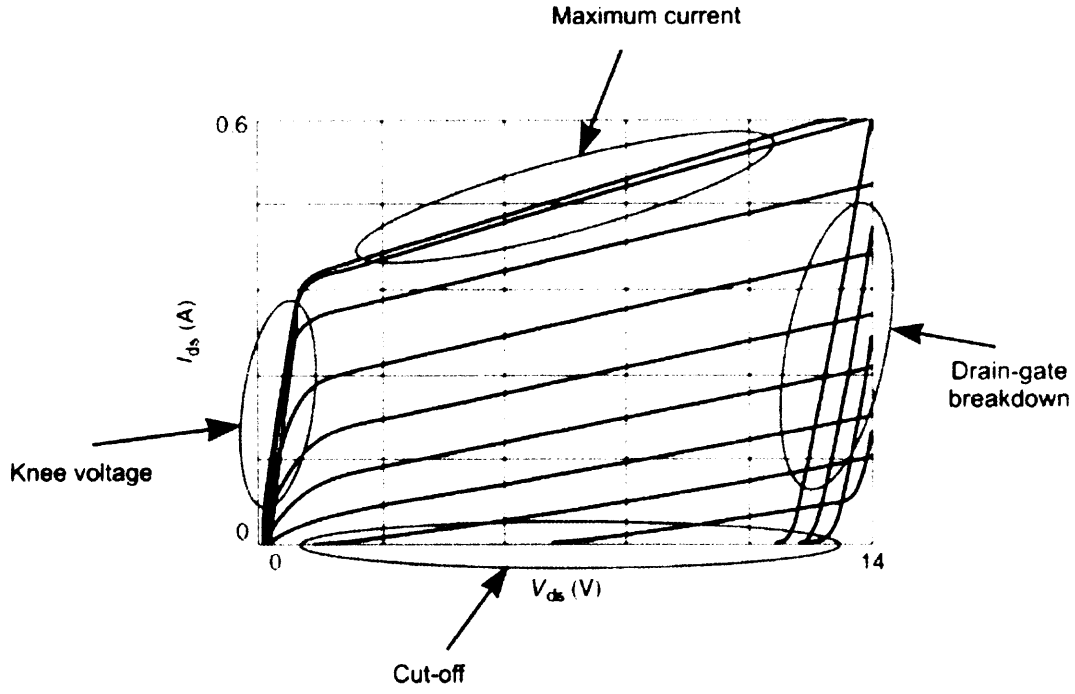

Figure 2.4 : Generic limiting non-linearities in FET transistor's output characteristics [1]

Figure 2.4 shows limiting non-linearities in the output characteristics of a transistor. This is due to the presence of the strong voltage-limiting and current limiting processes. In an FET, these are the cut-off, maximum current, drain-gate breakdown region and cut-off region. In principle, very little harmonics and distortion are generated until the strong linearities of the transistor are reached by the load curve [1].

Designing for high efficiency and high linearity together is very difficult, hence normally a compromise has to be under taken [4]. The practical way of achieving this particular goal with optimum performance for both linearity and efficiency is by doing proper transistor characterisation at the design stage of the amplifier.

2.2 RF Power Transistor Characterisations

Designing RF power amplifiers ideally involves using transistor models inside CAD software. The mathematical formulation of transistor non-linear model describes the relationships between the voltage waveforms and the current waveforms as they appear at the transistor terminals. The model is then used by the designer in a CAD simulator to predict the performance of any amplifier circuit containing the modelled transistor, even before the amplifier is actually built [5]. The designer can then optimise the RF power amplifier performance to meet the desired specification.

The most difficult part in transistor non-linear model formulation is to ensure the model represents mathematical relationship between voltage waveforms and current waveform behaviour that is consistent with the measured response. The fact that it is a model means that it has limitations and it is never perfect. Its accuracy depends on how the model is generated and how it can be verified within its limitations. The activity that can perform both the important functions of generating and verifying can be mostly accomplished using measured characteristics.

Since most of the power amplifiers operate in large signal environment, a measurement system suitable for characterising the power transistor under realistic conditions is desired. The "realistic" condition includes realistic stimulus and impedance environment. Realistic stimulus is a large signal with wideband multi-tone features. The impedance environment in large signal measurement system is provided by load-pull systems. The load-pull systems need to properly handle realistic stimulus for producing more accurate transistor models or validating transistor models to be used in power amplifier design.

2.3 Large Signal Multi-Tone Waveform Measurement System

Two important features in large-signal characterisation are [6]:

a) the availability of travelling waves (ab) as well as voltage-current (VI) representation

b) a unified approach for the frequency and the time domain

A comprehensive understanding of the device behaviour is only possible by looking into both signal representations [3, 6]. Large-signal measurement systems are able to convert the ab to VI waves and vice versa using the following equations:

$$a = \frac{V + Z_c I}{2\sqrt{Z_c}} \tag{2.2}$$

$$b = \frac{V - Z_c I}{2\sqrt{Z_c}} \tag{2.3}$$

$$V = (a+b) \bullet \sqrt{Z_c} \tag{2.4}$$

$$I = \frac{a-b}{\sqrt{Z_c}} \tag{2.5}$$

where Z_c is the characteristic impedance which by default has a value of 50 ohm.

A large signal measurement system normally uses very high frequency oscilloscopes in order of tens of GHz to sample the A and B waveforms [7]. The measured time-domain waveforms are then converted to frequency domain for analysis, error correction and data processing using the external PC connected to the oscilloscope. Figure 2.5 represents generic block diagram of Large Signal Time Domain measurement system.

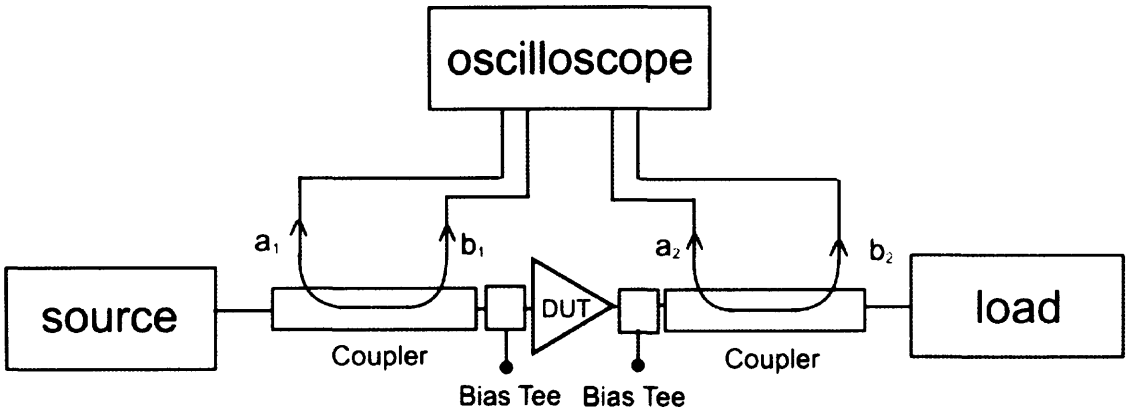

Figure 2.5: Generic block diagram of oscilloscope based large signal measurement system

Different types of sources or stimuli are being used in RF power amplifier characterisation and can generally be grouped as the following [8]:

a) One tone characterisation (CW)

b) Two tone characterisation

c) Multi-tone characterisation

d) Complex Modulation (e.g. WCDMA)

2.4 Importance of Impedance Matching in Power Amplifier Design

RF power transistor performance is a function of the following parameters [9]

a) Frequency

b) Input power

c) Quiescent bias

d) Modulation

e) Embedding Impedances

- Fundamental source impedances

- Fundamental load impedances
- Harmonic impedances of both sources and load
- Baseband impedances in DC paths

Thus in designing for a given specification it is necessary to determine the quiescent bias and embedding impedance. Efficiency, power, gain and distortion specifications are usually defined by the application.

If the power amplifier is driven by sufficiently small signals then S-parameters are normally capable of determining the necessary embedding impedances since the quiescent bias is unperturbed and inter-modulation distortions/harmonics are not important. Unfortunately when sufficiently large signals are present, S-parameters descriptions are not sufficient since device bias can be different from quiescent bias and the embedding impedances must account for harmonics and inter-modulation distortions components.

The experimental approach to determine the optimum embedding impedances for large signal operation is load and source pull. These approaches systematically vary the load or source impedances and allow direct measurement of device performance in real-time. Load pull is very important for the RF power amplifier designer. The main purpose of the power amplifier is to produce high power amplification and this behaviour is largely influenced by the load impedance.

2.5 Evolution of Load-Pull Measurement Systems

The basic method in load-pull measurements is to terminate the device under test (DUT) with adjustable impedances. Parameters such as power gain, output power, and DC to RF

power conversion efficiency are then measured as a function of input power level, device terminations and DC bias conditions [10]. The chief advantages of this approach are that the device is subjected to realistic operating conditions during the measurement and that the measured data can be used readily in the design cycle.

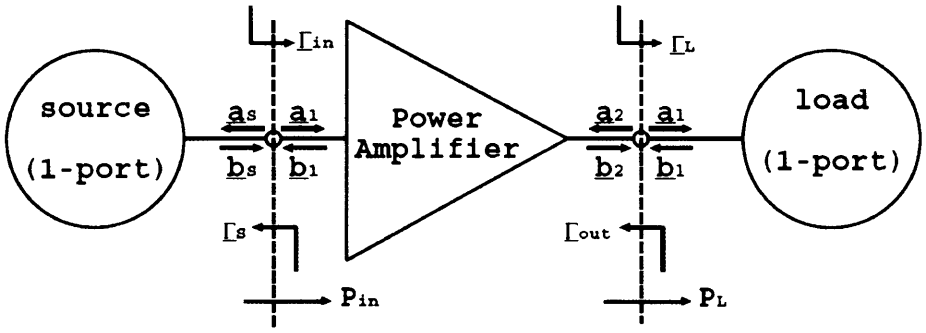

Figure 2.6: Power amplifier as a two-port network connected to source and load

Figure 2.6 shows the waves transmission around power amplifier. Based on this figure, the load reflection coefficient is given by

$$\Gamma_L = \frac{a_2}{b_2} \tag{2.6}$$

which determines the load impedance, Z_L, seen by the device

$$Z_L = Z_c\left(\frac{1+\Gamma_L}{1-\Gamma_L}\right) \tag{2.7}$$

with Z_c as the characteristic impedance.

In load-pull systems, the load impedance varies by experimental variation of the load reflection coefficient Γ_L. There are two main techniques being deployed for load-pull, namely passive and active load-pull. The main difference between the two techniques is

that while Γ_L is reflected naturally in passive load pull, it is reflected artificially in active load pull. From now on, the Γ_L will be referred to as Γ because the thesis is focusing on load-pull measurement.

2.5.1 Passive Load-Pull

Passive load-pull is the earliest form of load-pull, and normally it is performed using mechanical tuner albeit sometimes an electrical based tuner is used. Conceptually passive load-pull works similarly to circuit matching networks by changing the capacitance and inductance [3]. Traditionally the tuner is attached directly to the output of the DUT, but then for the oscilloscope to get the accurate measured information after the tuner it is necessary to perform a pre-calibration procedure that is complicated and time consuming. This is because the power loss of the tuner changes as it is tuned and the required information is at the DUT reference plane not at the measured tuner reference plane. The unknown tuner losses will introduce uncertainty into the measurement and these losses can be significant [10]. This can be resolved by performing a detailed calibration of the tuner at all its possible configurations. A better or "real-time" approach is to attach the coupler before the tuner to directly observe DUT behaviour thus the oscilloscope gets the appropriate measurement information [11]. A simple block diagram of a passive load-pull system with such a coupler configuration is shown in Figure 2.7.

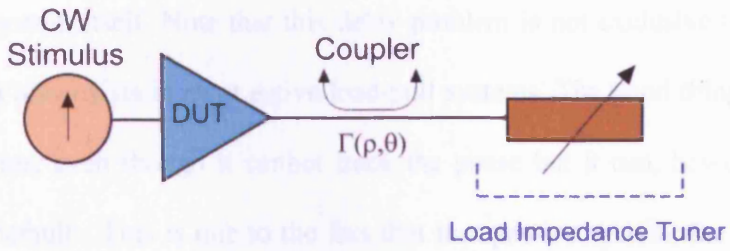

Figure 2.7: Passive load-pull

The placement of the coupler between the DUT output and the tuner, however, will results in non-zero physical length hence introduce extra loss and delay, therefore, the reflection gamma, Γ, will contain both loss and frequency variation. Recent advancements in RF coupler technology has significantly reduced the losses [11]. However, the effect of phase changes due to the distance between the DUT and tuner has not been sufficiently addressed [12,13]. This variation is further complicated by additional phase change within passive tuning systems. In order to demonstrate this problem, consider the variation of the Γ phase deviation ($\Delta\theta$) resulted from just 1 ns delay (Δt) that can be introduced by cable and measurement components along the Γ transmission and reflection. For a signal with a bandwidth (BW) of 10 MHz, the spread of Γ is as follows [13]:

$$\Delta\theta = \pm \pi \Delta t \, BW$$

$$\Delta\theta = \pm 1.8^\circ$$

As the modulation bandwidth goes up to 20 MHz (LTE and WIMAX), load-pulling up to third and fifth order inter-modulation distortions (IMD3 and IMD5) spans 100 MHz bandwidth. Using the same calculation method this can result in ±18° of Γ spread on the Smith chart. If this problem is not addressed when measuring non-linearity, it will be difficult to distinguish whether distortion is caused by the DUT or introduced by the

measurement system itself. Note that this delay problem is not exclusive to passive load-pull system but also exists in most active load-pull systems. The good thing about passive load-pull systems, even though it cannot track the phase but it can, however, tracks the amplitude by default. This is due to the fact that in a passive system, the reflected wave (a_2) is a function of the transmitted wave (b_2).

2.5.2 Active Load-Pull

In response to the fact that passive load-pull cannot cover the entire Smith chart, the RF and microwave measurement community has come up with active load-pull solutions in order to rectify the problem. The ability to provide open or short at the very edge of the Smith chart is of particular importance in load-pull investigation of high efficiency power amplifiers modes of operation such as class F and inverse class F. The main premise of active load-pull is that the DUT output is terminated with a match and then the active load-pull system generates the returning travelling wave a_2 hence synthesising the desired Γ. Thus any loss in the system measurement system can be actively compensated by the load-pull system.

The first generation of active load-pull uses open loop architecture. The open-loop architecture provides simplicity and the unconditional stability of the load-pull system [14]. The main disadvantages of open active load-pull are as follows:

a) Slow speed

b) Power dependence

c) Bias dependence

d) Bandwidth dependence

e) Stimulus unscalability

f) Load-pull target convergence iterations

Most of the problems are due to the fact in open loop load-pull system the reflected wave (a_2) is not a function of the transmitted wave (b_2). The speed suffers from the fact it needs many iterations in order to converge to a load-pull point on the Smith chart. Different power sweep levels for the same load-pull point will require a new iteration to converge and similar problems happened for different bias levels as well [15]. This is not a big problem for characterising a power amplifier with CW stimulus albeit the main disadvantage is a slower measurement time.

Multi-tone load-pull creates more fundamental problems. Firstly, modern power amplifier techniques that increase power amplifier efficiency, for example envelope tracking power amplifier, changes the bias according to the stimulus, therefore open loop load-pull architecture that cannot adaptively accommodate changing of bias point, hence is not usable for real-time measurement. Secondly, wireless standards that utilise constant amplitude such as GSM are being replaced by wireless standards that utilise amplitude and phase variation for better spectral efficiency. If the multi-tone system is representing a complex modulated signal with non-constant amplitude and phase, open loop active load-pull cannot track the stimulus. Furthermore since multi-tone stimulus has non-zero bandwidth, therefore, the load-pull system needs to give constant or controlled impedance across a particular bandwidth and for multiple bandwidths if tone spacing is varied. The task of ensuring an active load-pull can adaptively track the dynamic amplitude of complex modulation, giving constant impedance across a given bandwidth and for multiple

bandwidths still remains a major challenge. That is why most of the complex modulated measurement are performed using the more traditional passive load pull systems [16].

Consider the problem for the open active load-pull of stimulus scalability. Single tone (CW) stimulus requires a single RF generator for active load-pull that must be synchronised with the RF stimulus as shown in Figure 2.8.

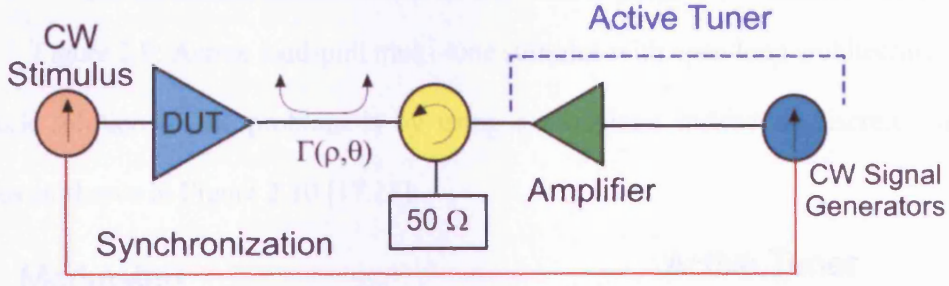

Figure 2.8: Active load-pull with CW stimulus

Suppose the number of stimuli is increased from just one to two. If the DUT goes into compression, non-linearity causes the distortions around the fundamentals signal. Significant distortions such as third order and fifth order inter-modulation distortions, IMD3 and IMD5, triple the total number of tones that need load-pulling to six. The increasing number of stimuli means increasing number of active load-pull sources. It increases the complexity of the system since each new load-pull source has to be synchronised with the stimulus. The matter is made even worse by the fact that in the non-linearity DUT operation, the distortion components that need load-pull do not exist in the stimulus as shown in Figure 2.9.

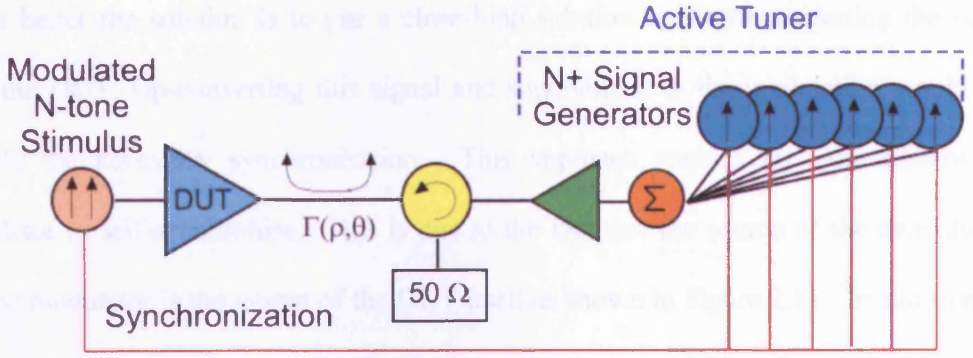

Figure 2.9: Active load-pull multi-tone stimulus with open loop architecture

A quick solution to the problem is by using a modulator instead of discrete load-pull sources as shown in Figure 2.10 [17,18].

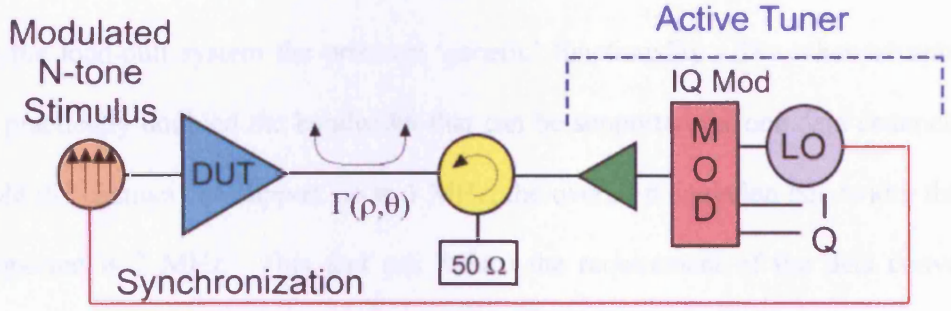

Figure 2.10: Active load-pull multi-tone stimulus with open loop architecture and modulator

This solution enables synchronisation of just the LO of the load-pull sources with the stimulus instead of each of load-pull sources. This reduces much of the complexity of the synchronisation but is still not a complete solution to the synchronisation problem. Similar to all previous active load-pull presented in Figure 2.8 and 2.9, it suffers from one major disadvantage of resorting to iteration for load-pull point convergence due to the emulated load-pull impedance is independent of the DUT output.

The better the solution is to use a close-loop solution by down-converting the output from the DUT. Up-converting this signal and supplying it to the modulation would thus provide the necessary synchronisation. This approach enables the demodulator and modulator to self-synchronise. This is due to the fact that the source of the demodulator and the modulator is the output of the DUT itself as shown in Figure 2.11. In addition this new load-pull architecture the emulated load-pull impedance is as a function of the DUT output, thus avoiding the slow and fuzzy iteration convergence.

The utilisation of in-phase and quadrature (IQ) signal at baseband has few advantages and one of them is that it can represents any signal from CW to the complex modulated, giving the load-pull system the precious 'generic' functionality. The other advantage is that it practically doubled the bandwidth that can be supported for one data channel. For example if I channel can support up to 1 MHz, the overall modulation bandwidth that can be supported is 2 MHz. This fact can reduce the requirement of the data conversion specification. This new promising self-synchronised architecture shown in Figure 2.11 is the foundation of a new load-pull technique entitled active envelope load-pull.

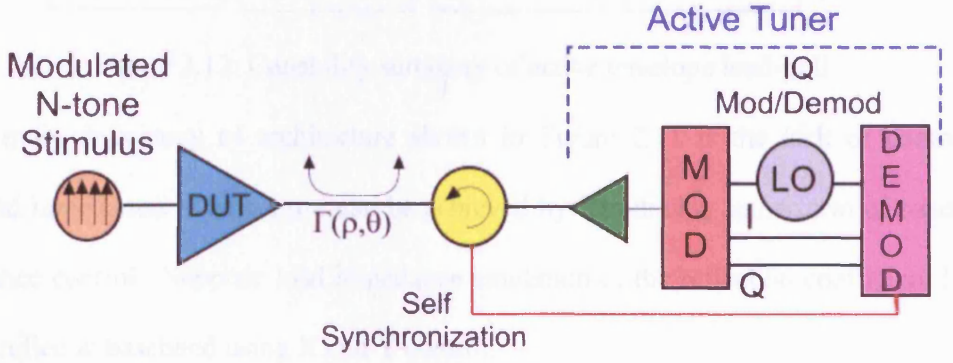

Figure 2.11: Active load-pull multi-tone stimulus with close loop architecture and demodulator/modulator

2.5.3 Active Envelope Load-Pull

The closed-lop active envelope architecture presented in Figure 2.11 can solve all of the problems of open-loop active load-pull mentioned in previous section. It is also much faster because no iteration is necessary for different power levels and bias points. The bandwidth independence and stimulus scalability provide critical functionality. Figure 2.12 summarises the major potential provided by the active envelope load-pull architecture.

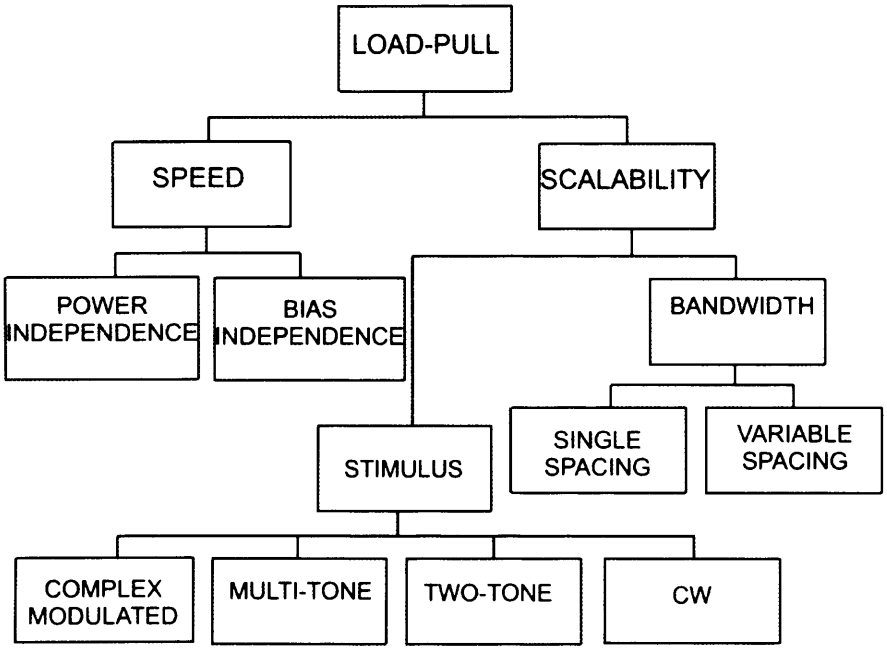

Figure 2.12: Capability summary of active envelope load-pull

The main deficiency of architecture shown in Figure 2.11 is the lack of control of emulated impedance. The control can be achieved by introducing some form of baseband impedance control. Suppose load impedance emulation or the reflection coefficient Γ can be controlled at baseband using X and Y control:

$$\Gamma = \frac{a_2}{b_2} = X + jY \tag{2.8}$$

At baseband the transmitted b_2 is given by Equation 2.9 and reflected a_2 is given by Equation 2.10:

$$b_2 = I + jQ \tag{2.9}$$

$$a_2 = I' + jQ' \tag{2.10}$$

Substituting Equation 2.9 and 2.10 into Equation 2.8 produce the following equations:

$$I' + jQ' = (I + jQ)(X + jY) \tag{2.11}$$

$$F(X,Y) = I' + jQ' = (XI - YQ) + j(XQ + YI) \tag{2.12}$$

From Equation 2.12, I' and Q' can be controlled separately as follows:

$$I' = XI - YQ \tag{2.13}$$

$$Q' = XQ + YI \tag{2.14}$$

Equation 2.12 indicates that it is a closed-loop system. This is due to the fact that the controlled load-pull output reflected to the DUT (I'/Q') is itself is a function of the DUT output (I/Q). The Γ amplitude and phase at baseband can be controlled according to the rectangular X and Y values based on Equation 2.13 and 2.14. Since the Smith chart is just another representation of rectangular plot, the control of the Γ is non-iterative and straight forward. Table 1 gives the relationship between the X and Y values combination with respect to the Γ points on the Smith chart.

Table 1: X and Y values combination with respect to the Γ points on the Smith chart

X	**Y**	**Γ amplitude**	**Γ phase**	**Termination**
0	0	0	0°	Match
1	0	1	180°	Open
-1	0	1	-180°	Short

Figure 2.13 provides the architecture of controllable active envelope load-pull using the rectangular X and Y values. If the control is performed via a computer, the user can set the value of the required Γ and the computer will then calculate the corresponding X and Y values on the behalf of the user. Initially an analogue based control unit has been developed for single tone (CW) [15] and recently extended to provide multi-tone stimulus capability [19]. There are scalability issues, both in terms of functionality and speed with the analogue control unit when increasing the bandwidth to more than 1 MHz. Hence, in this thesis a working alternative of a digital control unit was developed to complement and extend the analogue control unit capability [20]. It was developed using high speed digital signal processing of Field Programmable Gate Array (FPGA).

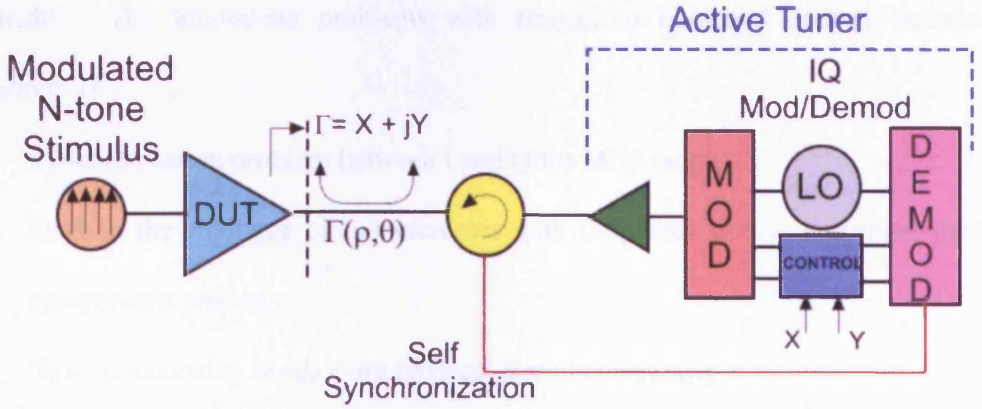

Figure 2.13: Active load-pull multi-tone stimulus with close loop architecture and demodulator/modulator including baseband control for impedance variation

2.6 Digital Control of Wideband Signal

As already stated, initially an analogue control system was used in the active envelope load-pull system since it is conceptually simple to implement. This approach worked well for CW and narrowband two-tone signals. Unfortunately as signal bandwidth increased

there is a limit to what analogue electronics can support without introducing distortion. Even though in active envelope load-pull system, the operating frequency is at down-converted baseband frequency and it is not at the much higher carrier frequency, the analogue approach can become troublesome. The new generation of modern wireless standards use much more modulation bandwidth (baseband) and as has been mentioned previously, the load-pull application has to support at least five times that bandwidth in order to cater for the effect of inter-modulations up to the fifth order. Thus the required operating frequency is in the range of hundreds of MHz or nano seconds (ns) range.

The active envelope load-pull architecture has more significant benefits for wide bandwidth applications. The analogue approach is struggling to scale to more than 1 MHz bandwidth. The immediate problems with respect to baseband control include the following:

i. Synchronisation problem between I and Q for MHz range
ii. Drift in the analogue circuit increases with frequency due to unwanted parasitic components property
iii. New functionality needs extra physical circuit complexity
iv. Reconfigurability is rather limited

In order to achieve the full potential of load-pulling for modern power amplifier characterisation with wideband multi-tone stimulus, it is important for load-pull to scale well. The first two mentioned problems are about scalability issues while the latter two are about functionality issues.

A few years back, digital systems was not attractive choice if you want to control high bandwidth RF modulated signals. Such signals pose a hefty performance requirement on

both of the data conversion and the signal processor. Fortunately due to the increased speed of the data conversion hardware (ADC and DAC), the prospect of using digital control is becoming more feasible [21].

After data conversion of analogue signal to digital, the digitised signals need to be processed accordingly. Real-time or low latency is a key requirement but the general purpose processors such as CPU and digital signal processing (DSP) processor cannot keep up with the speed. The specific purpose processors such as ASIC and ASSP can meet the requirement but lack the functionality and flexibility. A new breed of reconfigurable signal processor namely FPGA has been commercially available since 1980s that shows some promising high speed capability by utilising parallel processing technique similar to specific purpose processors but also has the functionality and the flexibility offered by general purpose processor. The combination of better data conversion hardware and faster signal processor offer promising capability of performing wideband signal control in the digital domain.

2.7 Chapter Summary

This chapter introduces the concept of load-pull and its evolution in the context of non-linear RF power amplifier characterisation. The main advantages and disadvantages of the popular load-pull concepts are described. The active envelope load-pull system is proposed as the solution for many of the problems existing in the conventional load-pull system. The proposed digital control for the new load-pull system can complement and further advance the capability of the new active envelope architecture.

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CHAPTER 3

DESIGN AND IMPLEMENTATION OF DIGITAL CONTROLLER

3.1 Processor Technology for Digital Signal Processing

The digital signal processing circuit performs tasks that in the past would have been implemented in the analogue system. Figure 3.1 shows a typical application used to implement an analogue system by means of digital signal processing (DSP) [1]. The analogue input is fed through an analogue anti aliasing filter whose stop band starts at half the sampling frequency f_s to suppress unwanted mirror frequency that occur during the sampling process. Then it is followed by analogue-to-digital converter (ADC) that is normally implemented with sample-and-hold and quantize (and encoder) circuit. The signal can be further processed or produce an analogue output signal via a digital-to-analogue converter (DAC).

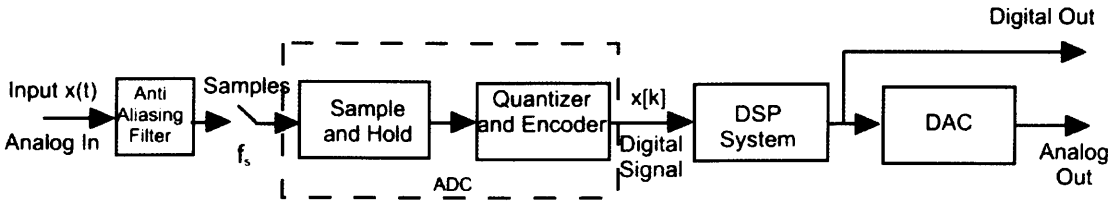

Figure 3.1: A typical DSP application [1]

For doing signal processing in hardware, there are few options that are available such as a general purpose processor (DSP/MPU) or specific purpose processor (ASIC/ASSP).

General purpose processors are very flexible because their architectures are optimized to process a fixed set of instructions but may not be ideally suited for a specific application, while specific purpose processor solution offer the ability to design a custom architecture that is optimized for a specific application. For example, a general purpose conventional DSP has only single multiply-accumulate (MAC) stage, so the computation must be executed sequentially, mainly in serial, but whereas an ASIC implementation can have multiple parallel multiply-accumulate (MAC) stages [2]. Comparing a general purpose processor versus a specific purpose processor it becomes apparent that the former offers slow speed but maximum flexibility (programmability) while the latter provides high speed with minimal flexibility. Alternatively, FPGA provides a compromise solution.

At the beginning of 21st century FPGA device families have several attractive features for implementing DSP algorithms. These devices provide fast-carry logic, which allows implementations of 32-bit (non-pipelined) adders at speeds exceeding 300 MHz, embedded 18 x 18 bit multipliers and large memory block [1]. FPGA combines the versatility of a programmable solution with the performance of dedicated hardware as shown in Figure 3.2 [3]. An FPGA can obtain the goal of parallel processing executing algorithms with the inherent parallelism due to the distributed arithmetic structure while avoiding the sequential instruction fetch and load/store bottlenecks of traditional Von Neumann architecture or "stored-program computer" [2]. DSP function in FPGA devices provide the following advantages as shown in Table 3.1 [4].

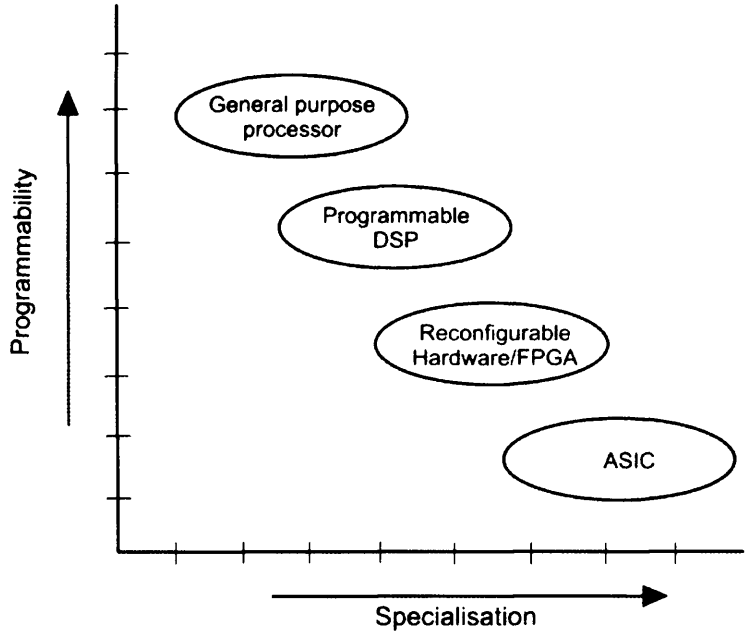

Figure 3.2: FPGAs offer both flexibility and performance [3]

Table 3.1: Comparison of FPGA and DSP processor [4]

Features	DSP	FPGA
Max Clock Rate	1 GHz	370 MHz
Max number of Multipliers	4 (16-bit X16-bit)	Over 700 18-bit X 18-bit (384 HW + 300 LE) OR Over 1400 9-bit X 9-bit
Max number of Instructions/Clock	4 or 8	100s to 1000s
Ease of Programming	C,C++ Software Flow	Hardware Description Language Hardware Flow
I/O Flexibility	Limited	Flexible
Memory Management	Built-In	Manual
Memory Bandwidth	1-Gbps SDRAM	9.5-Gbps DDRII
Power Consumption (For High-End Processing Devices)	Low Per Device (High Per Computation)	High Per Device (Low Per Computation)

Comparing to ASIC, FPGA disadvantages include generally slower, cannot handle as complex a design and draw more power. The advantages include a shorter time to market, ability to re-program in the field to fix bugs and lower non-recurring engineering costs. Vendors can sell cheaper and less flexible versions of their FPGAs which cannot be modified after the design is committed. The development of these designs is made on regular FPGAs and then migrated into a fixed version that more resembles an ASIC. Altera's fixed version is called Hardcopy. Altera is one of the two most popular FPGA vendors, the other is Xilinx. Together they both hold more than 80% of FPGA market share.

3.1.1 FPGA Fundamental

FPGA is a type of VLSI that is programmable and reprogrammable by using HDL code in "the field". It is a semiconductor device containing programmable logic components and programmable interconnects as shown in Figure 3.3 [1].

FPGA vendors similar to CPU companies have adopted two level hardware business strategy. The first level is the less expensive basic chip and the other level is more expensive high performance chip. Altera has *Cyclone* and *Stratix* while Xilinx has *Spartan* and *Virtex* for their basic and high performance version of their FPGA, respectively. In addition, Altera has *Hardcopy* while Xilinx has *Hardwire* for fixed version that resemble ASIC, as has been mentioned before.

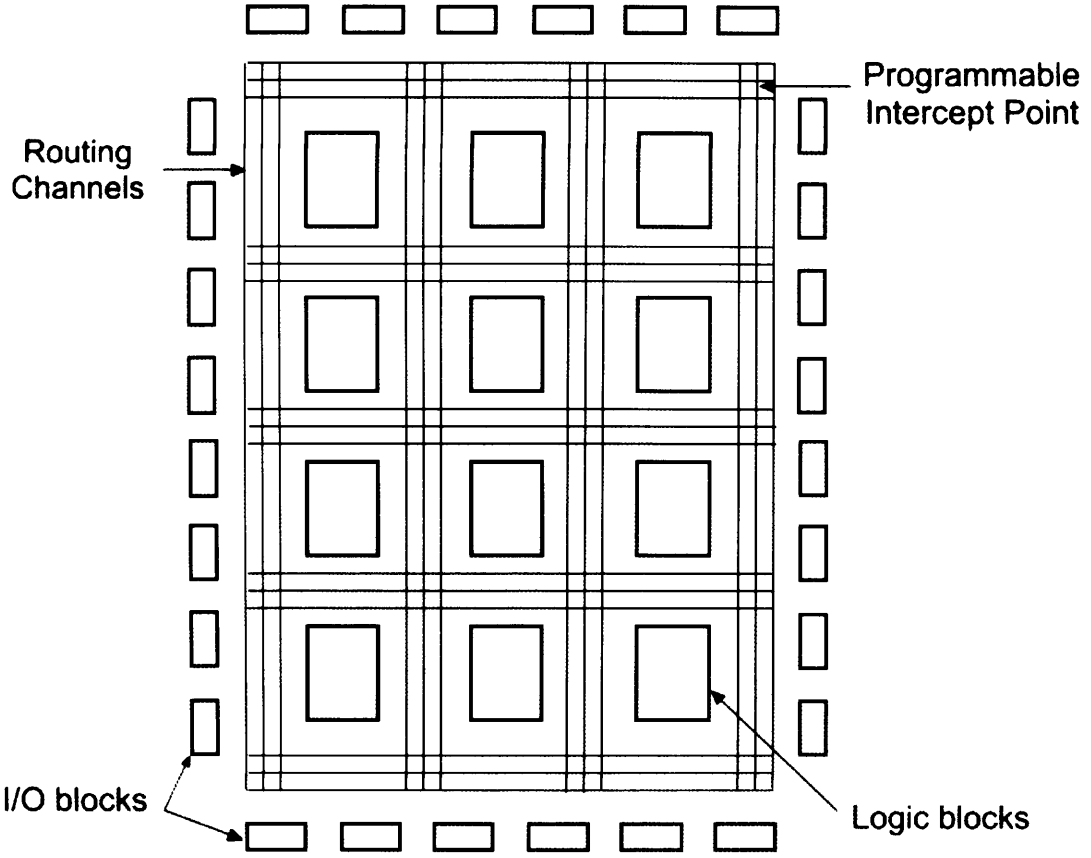

Figure 3.3: FPGA architecture [1]

The programmable logic components can be programmed to duplicate the functionality of basic logic gates such as AND, OR, XOR, NOT or more complex combinational functions such as decoders or simple math functions. These programmable logic components are referred as "logic block" and "logic element" by Xilinx and Altera, respectively. Figure 3.4 shows the basic programmable logic components and Table 3.2 shows its functionality.

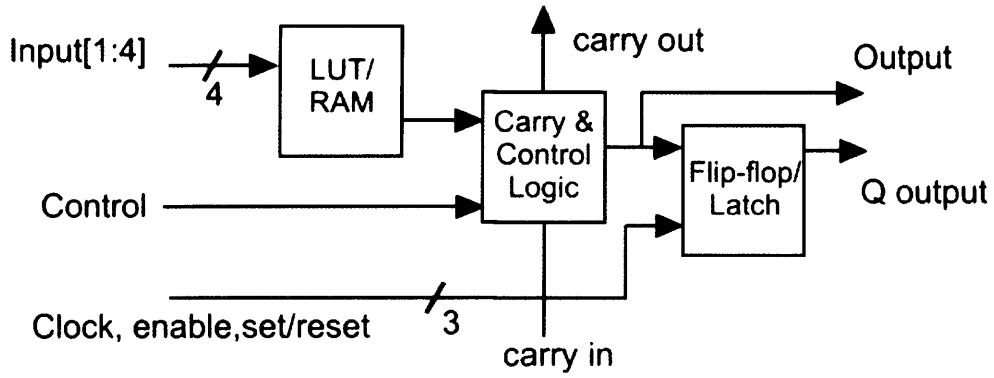

Figure 3.4: FPGA logic block or logic element [5]

Table 3.2: Functionality of logic block or logic element [5]

Components	**Functions**
Look-up Table	Truth Table
Memory Elements	Flip-flop/latch LUTs for small RAM
Carry and Control Logic	Fast adders/substractors

A hierarchy of programmable interconnects allows the logic blocks of an FPGA to be interconnected as needed by the system designer, similar to a one-chip programmable breadboard so that the FPGA can perform any required logical function. The program can be done after the manufacturing of the FPGA by the designer, hence the term "field programmable", i.e. programmable in the field.

There are two basic programmabilities of the FPGA, writing and changing configuration [5]. Writing configuration involves writing into the memory to define system function by configuring input/output cell, logic in logic block and connection between logic and input/output cells. Changing configuration is similar to writing configuration and it can change system function at anytime even while the system in

operation. The feature is very useful for dynamically changing the X and Y parameters or other control parameters of the active envelope load-pull digital controller without reprogram the whole FPGA. Altera called this feature as In-System Memory Content Editor (ISMCE). This particular feature enables a unique real-time and on-the-fly controlling ability without the need of CPU (hardware) and operating system (software) that can further complicate the design. The addition of the operating system will also add overhead for software context switching that can slow the controlling operation considerably.

3.1.2 Digital Signal Processing Using FPGA

FPGA can be viewed as a massive parallel computing system and it is also ideally suited for multi-channel DSP design that is normally found in modern wireless transceivers. FPGA allows many low sample rate channels to be multiplexed, for example TDMA, and processed in the FPGA at a high rate [1]. Similarly, the developed digital controller has two channels of in-phase (I) and quadrature (Q). Suppose the bandwidth of each channel is 10 MHz, therefore, the effective bandwidth supported by the digital controller is 20 MHz. Figure 3.5 shows the multi-channel parallel processing capability of FPGA.

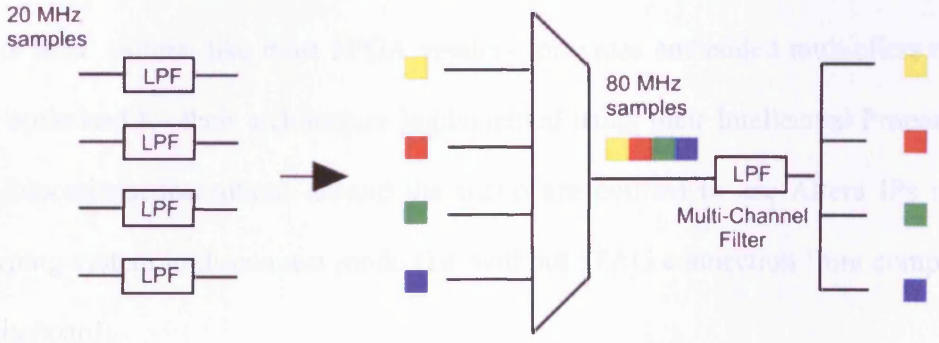

Figure 3.5: FPGA multi-channel parallel processing capability

DSP is a multiplication-intensive technology and to achieve high speeds, these multiplications operation must be accelerated. FPGA is well suited for DSP processing because a single FPGA processor can has several hundred embedded multipliers and a single FPGA processor can replace many DSP processors. Figure 3.6 shows a simple multiply-accumulate (MAC) of eight different inputs. The parallel MAC calculation is given in Equation 3.1. This equation has similar pattern with the main algorithms for the developed digital controller given in Equation 2.13 and 2.14.

$$Q = (AB) + (CD) + (EF) + (GH) \tag{3.1}$$

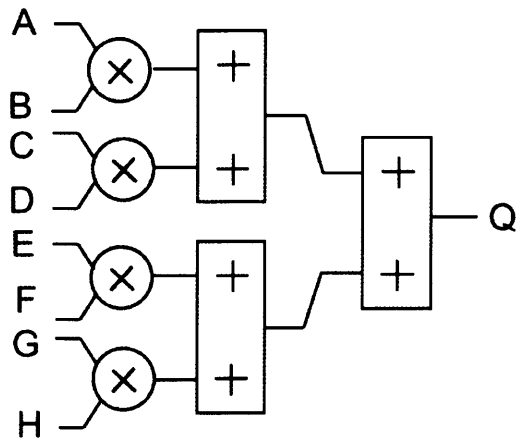

Figure 3.6: Fully parallel multiply-accumulate (MAC)

Figure 3.7 provides a number of trade-off options that can be performed with FPGA for speed or area. Altera, like most FPGA vendors, provides embedded multipliers that are highly optimised for their architecture implemented using their Intellectual Property (IP) [6]. Educational institutions around the world are entitled to use Altera IPs in their prototyping system in disconnect mode (i.e. without JTAG connection from computer to the main board).

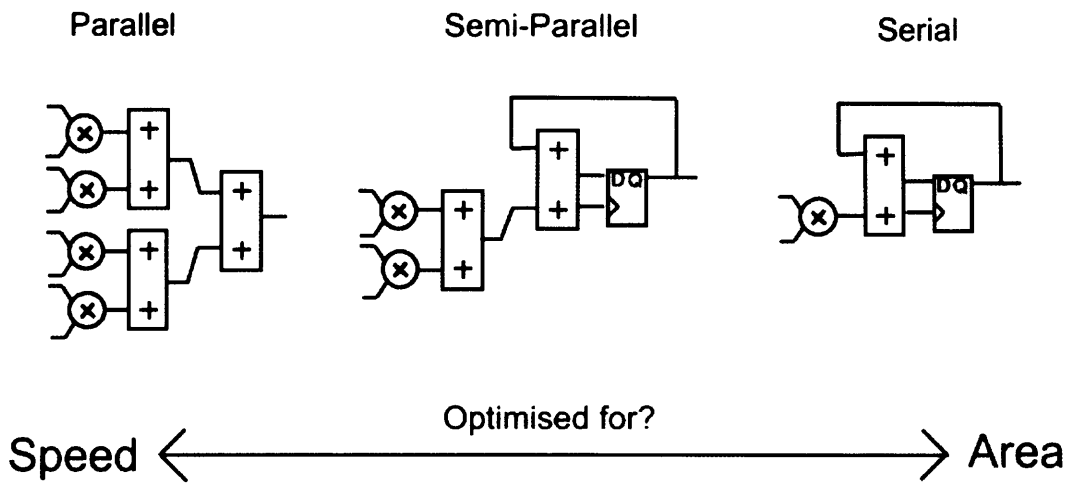

Figure 3.7: Optimising multiply accumulate (MAC) in FPGA

Altera devices have dedicated architectural features that make it easy to implement high performance multipliers. Altera's Stratix II devices, for example, contain embedded high performance multiplier-accumulate (MAC) in dedicated DSP that can operate at data rates above 300 million samples per second (MSPS) [6]. In addition to dedicated DSP blocks, it has memory blocks to implement high performance soft multipliers of variable depths and width. Developers, for example, can use the memory blocks as look-up tables (LUTs) that contain partial results from multiplication of input data with coefficients. For example, Stratix II device EP2S60 that is used in this project has 144 of multipliers for DSP blocks with (18 x 18) operating mode. It also has 325 Soft Multipliers with (16 x 16) operating modes giving the total number of 469 multipliers available.

Stratix II device EP2S60 has 36 DSP blocks that can be utilised according to the mode required by the developer. Table 3.3 shows the possible multiplier combinations. Each device has either the number of 9x9, 18x18 or 36x36 multipliers shown. Total number of

multipliers in DSP block for each device is not the sum of all multipliers.

Table 3.3: Possible multipliers combinations for EP2S60 device [6].

Device	DSP Blocks	9x9 Multipliers	18x18 Multipliers	36x36 Multipliers
EP2S60	36	288	144	144

Figure 3.8 shows the DSP block diagram operating modes and corresponding multiplication combination that can be utilised is shown in Table 3.4.

Table 3.4: Altera DSP block operating modes descriptions [4]

DSP Block Configuration Options	**Multiplication Combinations**
9- bit x 9-bit	8 Multiplies
	2 Multiplies With Accumulate
	2 sum of 2 Multipliers (Complex Multipliers)
	2 sum of 4 Multipliers
18- bit x 18-bit	4 Multiplies
	2 Multiplies With Accumulate
	1 sum of 2 Multipliers (Complex Multiply)
	1 sum of 4 Multipliers
36- bit x 36-bit	1 Multiply

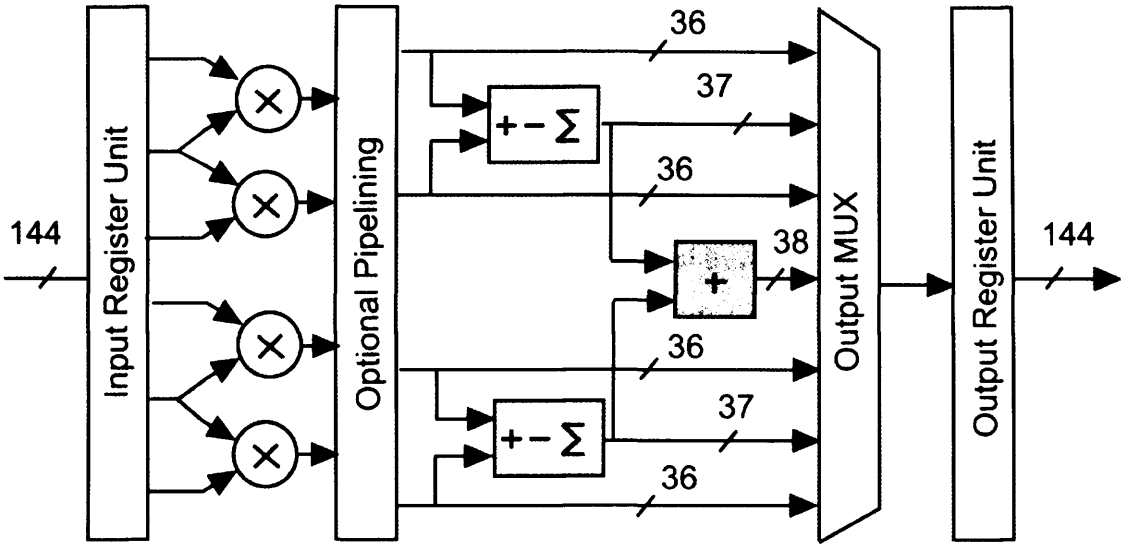

Figure 3.8: Altera DSP block operating modes [4]

3.1.3 FPGA Development Technique

Developing on a FPGA platform is quite unique since we are programming the hardware instead of software as in normal general purpose processor (CPU or DSP processor) development. The different nature of development requires a different style of thinking. For example, in FPGA development, timing is critical and timing analysis is part of the important design cycle. Furthermore, there is a subtle difference between programming for simulation and programming for implementation. Figure 3.9 shows the typical FPGA design cycle and Table 3.5 describes the corresponding cycle entity, regardless of the vendor. The final bitstream output is the configuration data to be loaded into a field programmable gate array (FPGA).

Table 3.5: FPGA design cycle descriptions [7]

Step	Description
Architecture design.	This stage involves analysis of the project requirements, problem decomposition and functional simulation (if applicable).
HDL design entry	The device is described in a formal **hardware description language (HDL)**. The most common HDLs are VHDL and Verilog.
Test bench	This stage involves writing of test environments and behavioral models (for verifying HDL description). .
Behavioral simulation	This is an important stage that checks HDL correctness by comparing outputs of the HDL model and the behavioral model.
Synthesis	This stage involves conversion of an HDL description to a so-called *netlist* which is basically a formally written digital circuit schematic. Synthesis can reveal some problems and potential errors that cannot be found using behavioral simulation.
Implementation	A synthesizer-generated netlist is mapped onto particular device's internal structure. The main phase of the implementation stage is *place and route* or *layout*, which allocates FPGA resources (such as logic cells and connection wires). Then these configuration data are written to a special file by a program called *bitstream generator.*
Timing analysis	During the timing analysis special software checks whether the implemented design satisfies timing constraints (such as clock frequency) specified by the user.

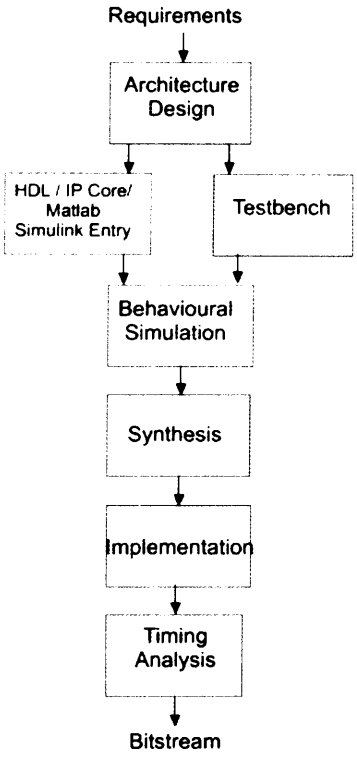

Figure 3.9: FPGA design cycle [7]

Conventionally design entry for FPGA is by programming totally in hardware description language (HDL) using Verilog or VHDL. Modern development for FPGA is a mash of programming techniques. Developers can choose any technique they are comfortable with or use combination of techniques. The lists of techniques that can be used are as follows:

i. Hardware description language (HDL)

ii. Vendors' Intellectual Property (IP) Cores

iii. Third Parties' Intellectual Property (IP) Cores

iv. Matlab Simulink Block Diagrams

v. Developers' Customised Block Diagrams

Utilising IP cores is the easiest way to design with, but it is the most inflexible while HDL is the hardest to design with but it is the most flexible. Most IP cores, however, are customisable to increase their flexibility. The most intuitive development is to design using top down design approach utilising schematics. The main schematic is the top level view of the design with block diagrams that can be any of the listed design entry techniques. Note that ultimately all design entries will be translated to HDL before being implemented.

Matlab Simulink is the latest trend for design entry as FPGA become more popular for DSP application implementation and prototyping platform. In this approach, Matlab wraps the vendors' IP and Matlab's IP cores in the Simulink block diagram. The premise of this approach is that since most DSP developers are already familiar with algorithms using Matlab programming environment, it should significantly reduce the learning curve of algorithm development and implementation. The main disadvantage is that for FPGA implementation and prototype programming, flexibility is limited to the available Simulink IP blocks [8]. In principle the developer can develop his/her own block but this will in turn require the knowledge of low level HDL programming that the originally targeted DSP developer was trying to avoid in the first place. From the author's point of view, the Matlab Simulink approach is good for first stage development with IP cores integration and evaluation in DSP system simulation.

In the early stage of the development, Matlab Simulink Block Diagrams utilising vendor's IP approach is used for prototyping the active envelope load-pull digital controller. After that, the digital controller is designed and developed using multiple design entry techniques including Verilog HDL, vendor's IP and customised block

diagrams. The development is done in Quartus II development environment. Quartus II is Altera's proprietary FPGA development environment that enables the full cycle of FPGA based implementation from design entry to bitstream as shown in Figure 3.9.

3.2 Controller Design and Implementation

The generic active envelope load-pull architecture measurement system (at the load side), regardless of the controller (analogue or digital) is given in Figure 3.10. The b_2 waveform from the output of the DUT is down-converted by the I/Q demodulator to a baseband quadrature pair of I and Q. The rectangular X and Y controls are then used to offset the quadrature pair to produce a new quadrature pair set. The new I and Q pair is then up-converted by I/Q modulator as a new a_2 waveform. Both of the demodulator and modulator are using the same local oscillator (LO) for synchronised operation. Essentially active envelope load-pull is a closed-loop active load-pull system with the active injection of a_2 reflected signal being the function of b_2 transmitted signal from the output of the DUT. The generic architecture of active envelope load-pull is shown in Figure 3.10.

The transmission and reflection planes attached to I/Q demodulator and modulator, respectively, are the same for both of the analogue and digital controllers. The main difference in the architecture is that digital controller requires ADC to convert the analogue signal to digital signal and DAC to do the reverse. The architecture of active envelope load-pull with digital controller is given in Figure 3.11.

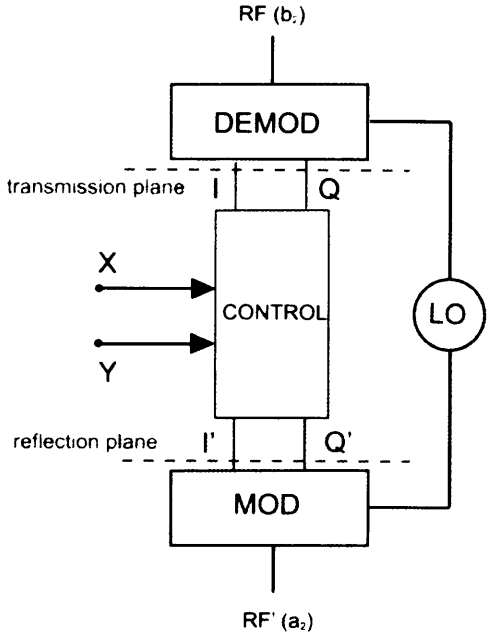

Figure 3.10: Generic active envelope load-pull architecture

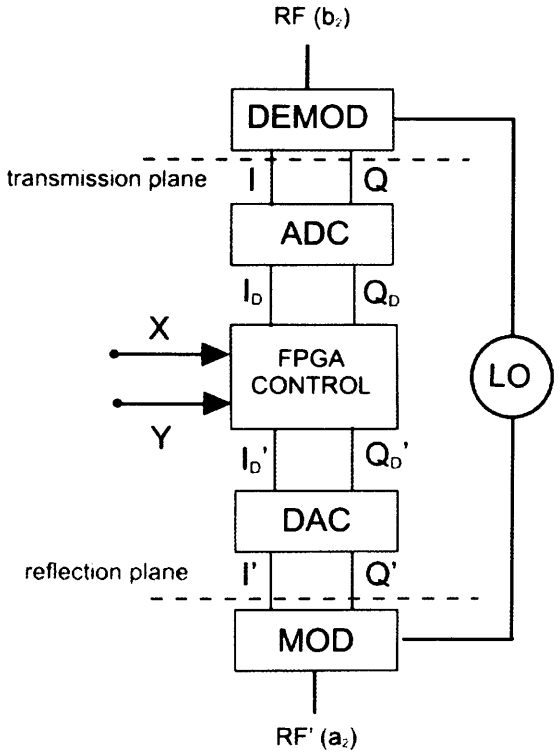

Figure 3.11: Digital controlled active envelope load-pull architecture

3.2.1 Digital Controller Design

As a minimum the digital controller must have the same basic functionality as the analogue control. The improved potential of having more bandwidth with the digital controller is that it can provide robust wideband investigation of power amplifier and transistor for modern wireless standard. In addition it should provide better insight into the effect of impedance variation on the power transistor performance.

The complete proposed digital controller should be equipped with the following basic controlling functionalities to cover the entire Smith chart:

i. Complex multiplier

ii. Amplitude scaler

iii. Polarity inverter

The complex multiplier is to implement the main algorithm given in equation 2.13 and 2.14. The amplitude scaler is to provide full coverage of the Smith chart. The polarity inverter is to change the polarity of X and Y control for different quadrants of the Smith chart.

Additional control functionalities are as follow:

iv. Delay compensator

v. 10 MHz synchronisation

The delay compensator task is to delay and align the reflected a_2 waveform with regard to the transmitted b_2 waveform. Any non-zero delay will result in delay spread or impedance variation centred in the middle of Smith chart. As modulation frequency increases, the spread will increase accordingly. This phenomenon exists in both active

and passive load-pull. It is theoretically possible to compensate the delay with active load-pull technique whereas it is impossible with passive load-pull. This is due to the fact that passive architecture does not actively inject signal back to the DUT.

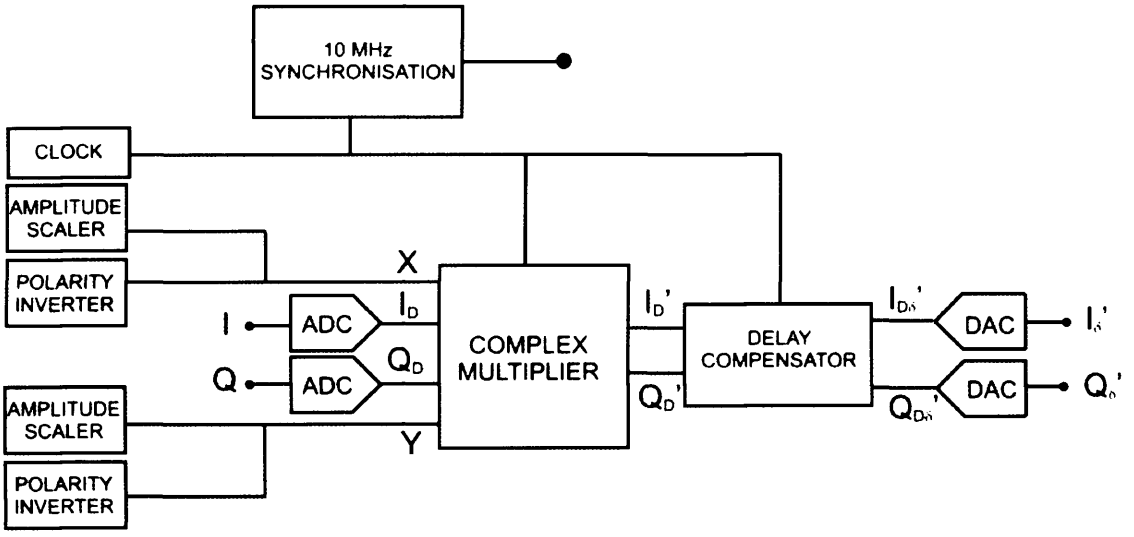

Figure 3.12: Digital controller architecture

Table 3.6: Digital controller I/Q signals descriptions

Quadrature Signals	Description
I	In-phase (I) analogue signal from the demodulator
Q	Quadrature (I) analogue signal from the demodulator
I_D	Digitised in-phase signal
Q_D	Digitised quadrature signal
I_D'	Modified digitised in-phase signal
Q_D'	Modified digitised quadrature signal
$I_{D\partial}$'	Delay compensated modified digitised in-phase signal
$Q_{D\partial}$'	Delay compensated modified digitised quadrature signal
I_∂'	Delay compensated modified analogue in-phase signal
Q_∂'	Delay compensated modified analogue quadrature signal

The 10 MHz synchronisation can be set up as the source of synchronisation to the rest of measurement system instrument e.g. oscilloscope, source, etc. This can help reduce the phase drift of the digital controller with respect to the measurement system. The proposed architecture of the FPGA based digital controller is shown in Figure 3.12 and the I/Q signal explanations are given in Table 3.6.

As has been mentioned before, the digital controller was designed using Quartus II software available from Altera. Quartus II is a one stop solution for doing small to medium sized FPGA projects. It covers the entire FPGA design cycle given in Figure 3.9.

3.2.2 Digital Controller Implementation

As has been mentioned before the digital controller can be divided into a few logical functional blocks. In addition to these blocks, the design has signed to unsigned conversion for DAC data output. The complete list of the blocks being implemented inside the digital controller are as follows:

i. Complex multiplier
ii. Amplitude Scaler
iii. Polarity inverter
iv. Delay compensator
v. 10 MHz synchronisation
vi. Signed to unsigned conversion

The equivalent Quartus II design for Figure 3.12 is given in Figure 3.13 and the control flow-chart is given in Figure 3.14. In Figure 3.13 the top level design schematic includes collection blocks of Verilog HDL and Altera IP. The design has hierarchical structure for

easier organisation. It also contains custom blocks that encapsulate other blocks. Most of the block components, including the ADC and DAC, are clocked at a common 100 MHz signal. Note that the data signal ADC is in signed format while the data signal output from the DAC is in unsigned format. The data signal format and conversion hence need to be dealt with accordingly.

i. Complex multiplier

The main blocks are the complex multiplier blocks that implement equation 2.13 and 2.14. The complex multiplier utilises Stratix II firm multipliers that can use a combination of DSP blocks and logic resources as required based on the operation mode [6]. Specifically it uses customisable *altmult_add megafunction* that utilises Altera IP to implement the complex multipliers. The megafunction optimised on performance and FPGA resources for performing the multiplications.

There are two blocks being used, one for equation 2.13 and another for equation 2.14. Figure 3.15 depicts the first complex multiplier implementing equation 2.13 encapsulated inside the complex multiplier block in Figure 3.12. The *megafunction* performs substraction for both of the multiplication results. The block implementation of equation 2.14 is similar to Figure 3.15 except that the megafunction performs addition instead of substraction for both of the multiplication results. Both of the complex multiplier blocks are synchronised with the entire design with the 100 MHz clock.

All input and output of the multipliers are signed in this design. The megafunction, however, is quite flexible in that it can support both signed and unsigned input/output. Each multiplication input has 12 bits and overall complex multiplication output is 32 bits.

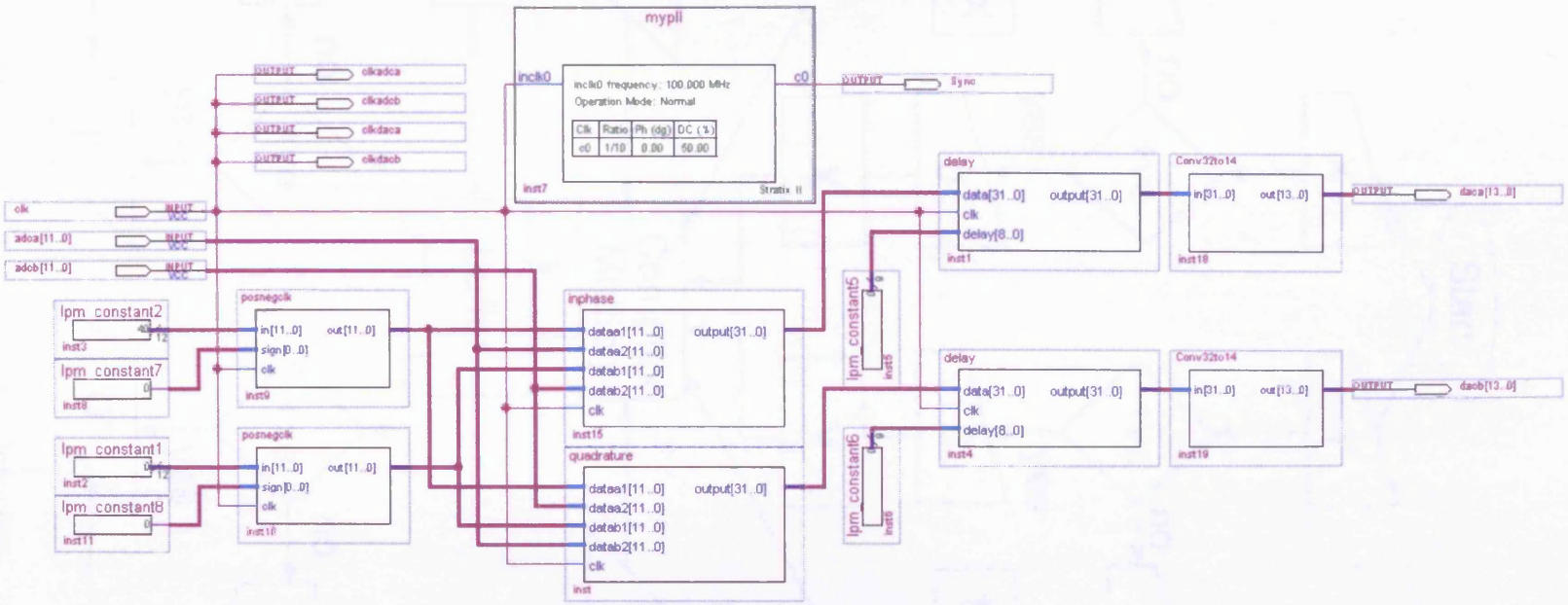

Figure 3.13: Digital controller top-level schematic

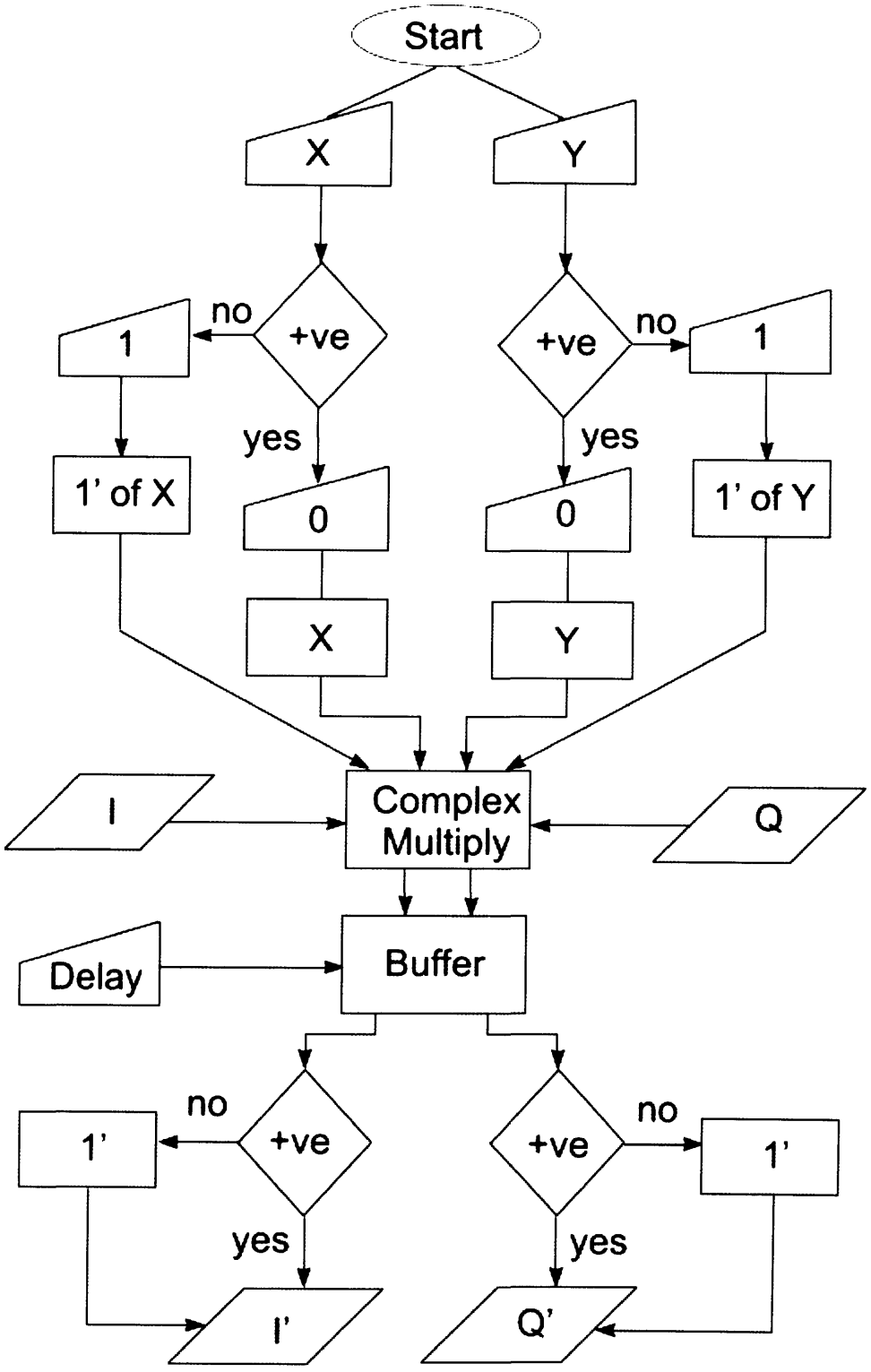

Figure 3.14: Digital controller flow-chart

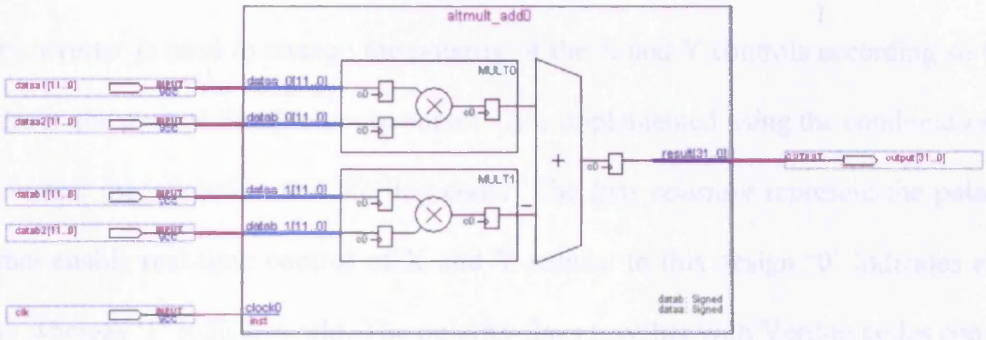

Figure 3.15: Complex multiplier implementation using *altmult_add megafunction*

ii. Amplitude Scaler

The amplitude is used to scale to the edge of smith chart and it utilised *lpm_constant* IP core from Altera. This constant can be changed or reconfigurable dynamically after the FPGA is programmed. This feature is very important for the active envelope load-pull for varying the Γ in real-time by manipulating the X and Y values. This feature must be enabled by clicking the "Allow In-System Memory Content Editor to capture and update content independently of the system clock" as shown in Figure 3.16.

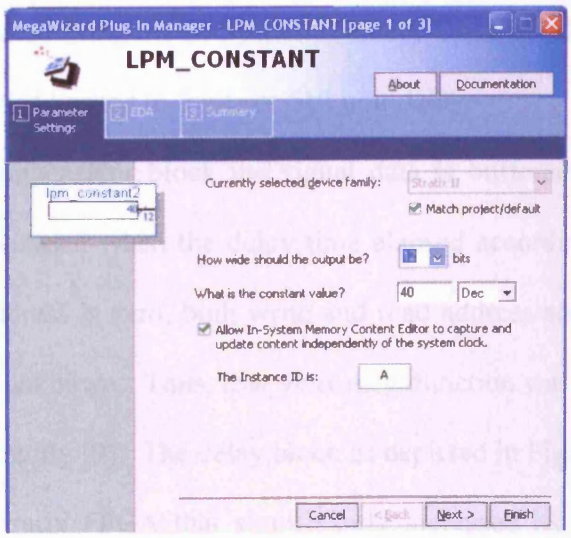

Figure 3.16: Configuration for lpm_constant with ISMCE option

iii. Polarity inverter

Polarity inverter is used to change the polarity of the X and Y controls according so that Γ resides in the desired Smith chart quadrant. It is implemented using the combination of *lpm_constant* megafunction and Verilog code. The *lpm_constant* represent the polarity flags that enable real-time control of X and Y values. In this design '0' indicates even polarity whereas '1' indicates odd. The polarity flags together with Verilog codes convert the scaler polarity accordingly as shown in Appendix A.

iv. Delay compensator

In FPGA or digital circuits, delay block can be implemented using several techniques. Two commonly used techniques are the chain of D flip-flops or the memory based technique, and this project utilised the memory based technique. Note however that both of these techniques implement unit delay or multiples of unit delay, not fractional delay. In this design, a unit delay equals to 10 ns i.e. corresponding to 100 MHz clock frequency. The delay constant is again implemented in *lpm_constant* megafunction that can be dynamically varied using the In-System Memory Content Editor (ISMCE) feature. In this design the delay is limited to 9 bits or 512 unit delay.

Inside the delay compensator block the signal data is buffered inside a memory or RAM and it is only released when the delay time elapsed according to the entered unit delay. If the delay address is zero, both write and read address are the same, hence the output of the RAM is unknown. Thus, *lpm_mux* megafunction was added to allow delay of zero to function correctly [9]. The delay block as depicted in Figure 3.17 utilises built-in RAM inside the Stratix FPGA that significantly increased its performance. Using external RAM will add more latency to the delay block.

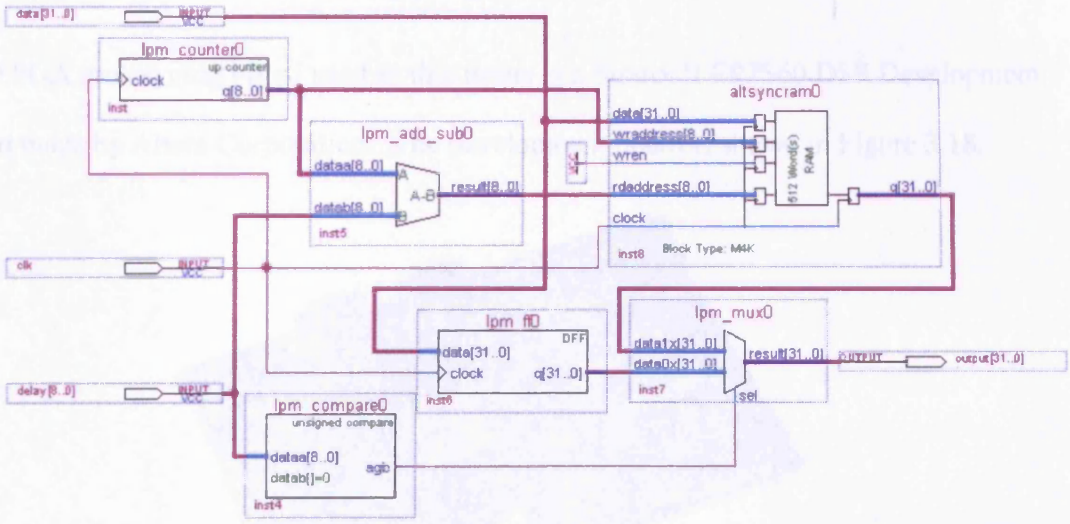

Figure 3.17: Delay block implementation

v. 10 MHz synchronisation

The 10 MHz can be added to the design by utilising digital Phase Locked-Loop (PLL). Altera provides customisable PLL megafunction that can provide phase synchronisation and frequency division at the same time. The input of the PLL is the 100 MHz clock signal and the output is the phase synchronised 10 MHz signal that can be linked to the rest of the measurement system. This fact is reflected in the Figure 3.13 with a ratio of 1/10 in the PLL configuration.

vi. Signed to unsigned conversion.

Before the data signal is output to the DAC, the systems needs to convert the signal from signed to unsigned since the DAC only accept unsigned format. The Verilog codes that perform this signed to unsigned format is given in Appendix B.

3.2.3 Digital Controller Prototyping

The FPGA prototyping board used in this thesis is a Stratix II EP2S60 DSP Development Board made by Altera Corporation. The development board is shown in Figure 3.18.

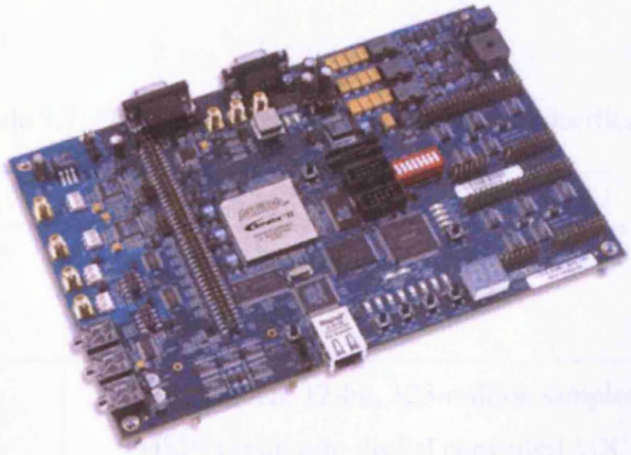

Figure 3.18: DSP FPGA development board by Altera

The development board comes with plethora hardware and peripherals. Not all of them are being used in this project, for examples, an RJ45 Ethernet networking jack and a stereo audio coder/decoder (CODEC). Table 3.7 summarise that main hardware specifications of the board that are relevant to this thesis.

Two of the most important hardware elements for the implementation are the ADCs and DACs. Each of the ADCs and DACs has jumper for the clock that need to be set up correctly. When implementing the design in the schematic as shown in Figure 3.13, FPGA clock and input/output need to be connected properly to their respective board pins. This can be performed using the pin assignment menu available from the Quartus' *Assignment* menu. For example the assign clock input is connected to pin AM17 according to the data sheet [10]. Similarly the 10 MHz synchronisation output is

connected to pin R30 that is located next to the ground pin in the 40 pins connecter. Thus it is easy to connect two wires to carry the 10 MHz signal for synchronising with other equipments. The ADCs and DACs pins are also connected accordingly. The configured pin locations for ADCs and DACs are given in the Appendix C and Appendix D, respectively.

Table 3.7: DSP development board hardware specifications

Hardware	Description
FPGA	• Stratix II EP2S60F1020C4 device
Analog I/O	• Two-channel, 12-bit, 125-million samples per second (MSPS) analog-to-digital converter(ADC) • Two-channel, 14-bit, 165-MSPS digital-to-analog converter (DAC)
Digital I/O	• JTAG connector • Two 40-pin prototype expansion connectors
Cables and accessories	• USB-Blaster download cable • Power supply
External clock source	• Socketed 100 MHz Crystal oscillator

All the files related to the design in figure 3.13 are kept under a single project. The project is then compiled. The compilation process performs the synthesis, implementation and timing analysis as described in Figure 3.9 and Table 3.5. If there is

no outstanding error, the compilation is successful. The bitstream generated from the compilation process is used by the Quartus programmer to program the FPGA device using USB-Blaster via the JTAG interface. Once programmed the FPGA can operates stand alone without a connection to the PC. Normally the JTAG connection is left connected with the PC for changing the X and Y values dynamically in real-time.

When performing load-pull using the digital controller there are two Quartus' programs that are useful. They are Signal Tap Editor (STP) and In-System Memory Content Editor (ISMCE). The STP is a real-time logic probing utility for the FPGA. Basically when there is an STP file in the project, part of the logic resources inside the FPGA is being used as a logic probe. The binary data in STP can be presented in many formats but the most useful for the load-pull is to represent the data as the time domain waveforms. Essentially, the waveforms view is what we expect on an oscilloscope display. Figure 3.19 shows the snapshot of digital time domain waveforms for the ADCs input and the DACs output while performing an actual load-pull of a power transistor with a two-tone stimulus.

The ISMCE is the interface for changing dynamically the value of X and Y. Based on Figure 3.20 there are six constants that can be varied as follows:

i. Scaler A and B for I and Q, respectively.

ii. Polarity inverter flag S1 and S2 for I and Q, respectively.

iii. Delay compensation D1 and D2 for I and Q, respectively.

Step (i) and (ii) enable the X and Y values to cover the entire Smith chart. Step (iii) compensates the delay inside the closed loop of active envelope load-pull. Note the values are in hexadecimal numbers.

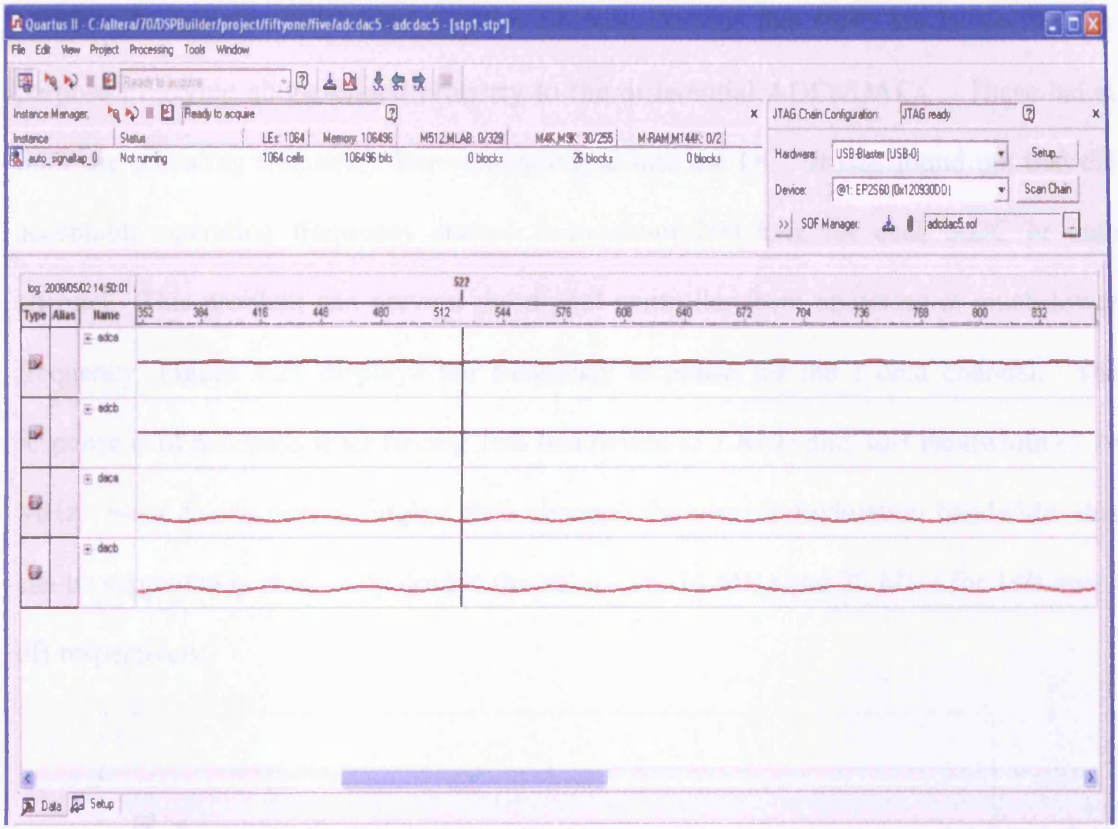

Figure 3.19: STP display waveforms of ADCs input and DAC output

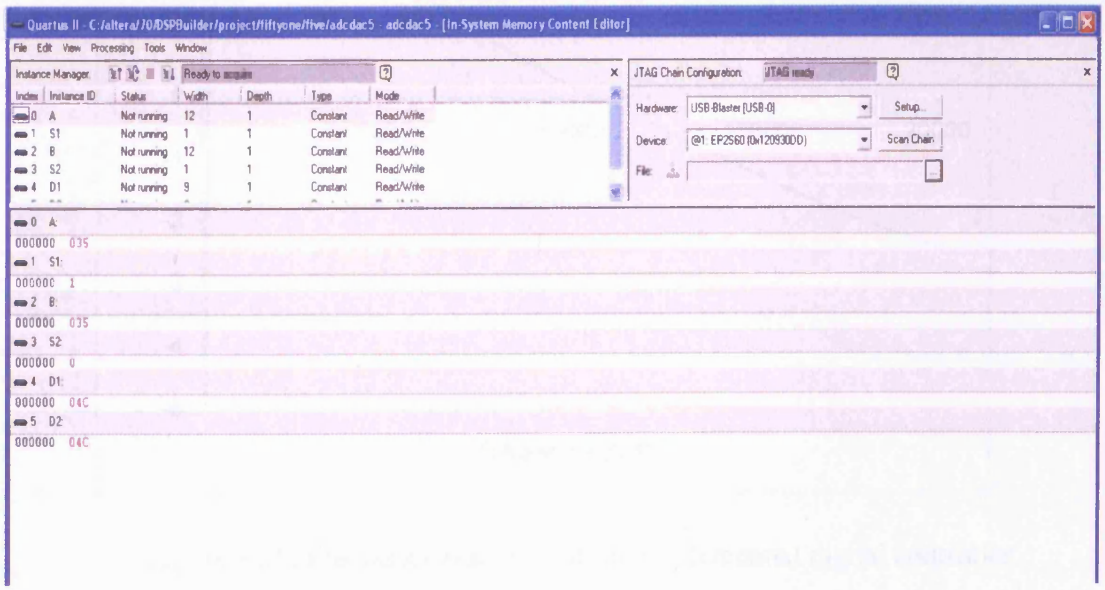

Figure 3.20: ISMCE for real-time control of X/Y values and delay compensation

While testing the ADC input it soon become obvious that there are baluns for the purpose of giving single-ended property to the differential ADCs/DACs. These balun limit the operating frequency from extending to into the DC. It was found out that the acceptable operating frequency started from about 200 kHz for each ADC or data channel. This problem can prevent the digital controller from operating at much lower frequency. Figure 3.21 displays the frequency response for the I data channel. The response is of bandpass filter having 1dB bandwidth of 7 MHz and 3dB bandwidth of 10 MHz. Since this is only a single I data channel, the overall modulation bandwidth that can be supported is practically double the values i.e. 14 MHz and 20 MHz for 1dB and 3 dB respectively.

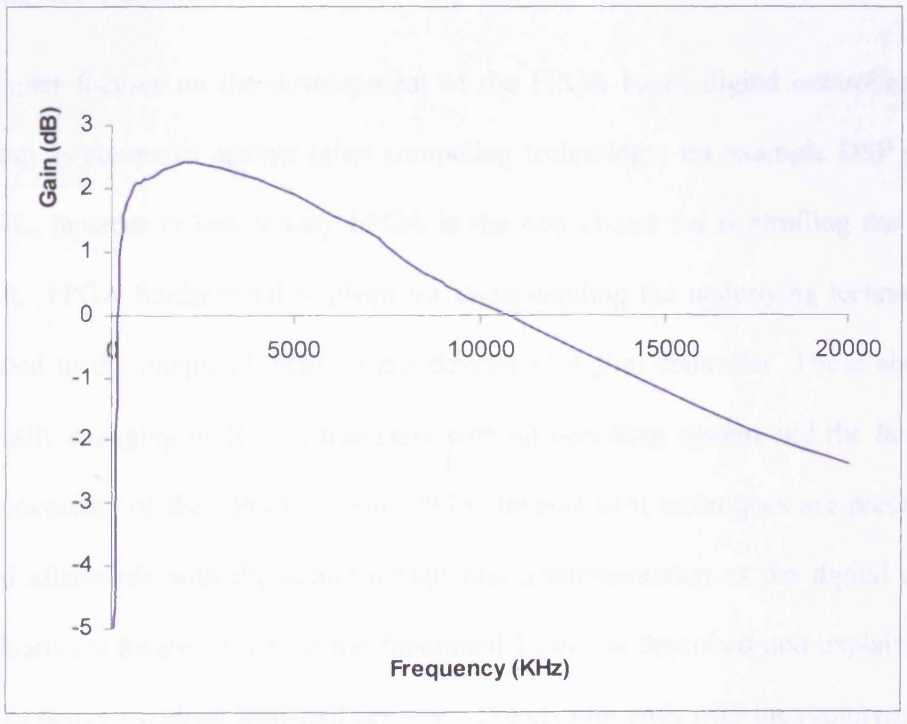

Figure 3.21: Frequency response of the implemented digital controller

From the compilation summary, the total utilisation of FPGA resources can be determined as depicted in Table 3.8 and total utilisation is less than 10%.

Table 3.8 Stratix II FPGA hardware resource usages

Hardware Resources	Number of logic element
Combinationals ALUTs	649
Dedicated Logic Registers	1,327
Total pins	63
Block Memory Bits	124,928
DSP block (9-bit elements)	8
PLL	1

3.3 Chapter Summary

This chapter focuses on the development of the FPGA based digital controller. FPGA technology is compared against other competing technology, for example DSP processor and ASIC, in order to justify why FPGA is the best choice for controlling the envelope load-pull. FPGA fundamental is given for understanding the underlying technology that contributed to the unique abilities of the developed digital controller. These abilities are dynamically changing of X /Y parameters without operating system and the fast parallel signal processing of the FPGA. Then FPGA development techniques are presented and followed afterwards with the actual design and implementation of the digital controller using Quartus software. Each of the functional blocks is described and explained in the context of active envelope load-pull activity. The chapter ends with the prototyping of the digital control using the FPGA development board. FPGA hardware resource usages of the implementation and the frequency response of the digital controller are determined.

3.4 References

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CHAPTER 4

VERIFICATION OF WIDEBAND MULTI-TONE ACTIVE ENVELOPE LOAD-PULL

4.1 Load-pull and Multi-tone Measurement System Integration

A generic block diagram of digital sampling oscilloscope (DSO) based large signal measurement system with load-pull system for power transistor characterisation is given in Figure 2.5 inside Chapter 2. Essentially the multi-tone measurement system has the same basic architecture but requires an RF source that can generate multi-tone waveforms and load-pull that can control the multi-tone stimulus. Multi-tone RF source is not a problem, and it can be purchase off-the-shelf for modulation bandwidths of more than 100 MHz. Load-pull systems, passive-or active, have difficulty in keeping up with the high modulation bandwidth of the multi-tone RF source as explained in Chapter 2. The main focus of the thesis is to design and develop a load-pull system that can support wideband multi-tone RF source or stimulus for power transistor characterisation.

Figure 4.1 presents active envelope load-pull integrated with the multi-tone measurement system. From the multi-tone measurement system point of view, the *load side* is the same regardless of the load-pull system being used. The actual measurement system has switches for RF signal flow regulation but they are not included in the figure for the sake of simplicity. For example a specific combination of switch configurations

can cause the load side to match 50 ohm impedance or the impedance set up by the load-pull system. For normal measurement the RF signal flows from the source to the load through the device-under-test (DUT). The travelling waveforms are picked up by the directional coupler and presented to the Digital Sampling Oscilloscope (DSO). Eventually the data is passed to PC for further processing and error corrections. In addition to processing and displaying the measurement data, the PC is also used to control measurement instruments such as the RF source for automated measurement capability such as sweeping the source power.

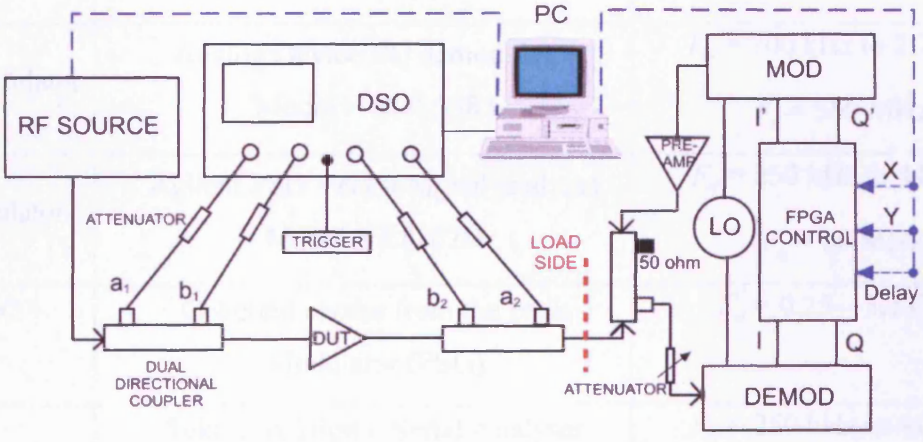

Figure 4.1 Active envelope load-pull integrated with multi-tone measurement system

The digital control implementation using FPGA of active envelope load-pull has been described in Chapter 3. There is a directional coupler, similar to coupler being used by the oscilloscope, that separates the transmitted and reflected waveforms of b_2 and a_2, respectively. The FPGA platform can only handles low frequency and low power signal levels. The low frequency is provided by the down-conversion of the transmitted RF waveforms (b_2) signal by the I/Q demodulator whereas the low power is provided by the attenuator. After the processing is performed by the FPGA, the signal needs to be up-

converted and amplified for producing comparable reflected RF waveforms (a_2) by the modulator and pre-amplifier, respectively.

Table 4.1: Multi-tone Active Envelope Load-pull Measurement System Components

Hardware Instruments	**Descriptions**	**RF frequency = F_{rf}** **Modulation freq = F_m**
RF source	Agilent PSG Vector Signal Generator Model = E8267D	F_{rf} = 250 kHz to 44 GHz F_m = 80 MHz
Directional Coupler	Krytar 10 dB directional Coupler Model = 1820	F_{rf} = 1 GHz to 18 GHz
Demodulator	Analog Device I/Q demodulator Model = ADL5382	F_{rf} = 700 kHz to 2.7 GHz F_m = 500 MHz
Modulator	Agilent PSG Vector Signal analyzer Model = E8267D	F_{rf} = 250 kHz to 44 GHz F_m = 80 MHz
LO	Coherent carrier from the back Modulator (PSG)	F_{rf} = 0.25 – 3.2 GHz
Oscilloscope	Tektronix Digital Serial Analyser Model = DSA 8200	F_{rf} = 250 kHz to 44 GHz
FPGA board	Stratix II DSP Development Kit Model = EP2S60	F_m = 20 MHz
Pre-Amp	HP83020A Microwave Amplifier Model = 83020A	F_{rf} = 250 kHz to 44 GHz
Attenuator	Mini-Circuits 30 dB Attenuator Model = VAT-30+	F_{rf} = DC to 6 GHz
Trigger	Agilent Arbitrary Waveform Generator (AWG) Model = 33250A	F_{rf} = 80 MHz

Table 4.1 shows the descriptions of components used in the active envelope load-pull measurement system. Most of the instruments are controlled by the PC using GPIB interface and the FPGA board is controlled using USB-to-JTAG (USB-Blaster) interface.

4.2 Configurations and Power Budget for Active Envelope Load-pull

Unlike passive load-pull, active load-pull must be configured properly and power budget must be calculated before the measurement take place. This is because it is possible to give more power than the RF source. If Γ is outside the Smith chart, the DUT can go into oscillation and probably be degraded. Figure 4.2 shows the power budget for the measurement and characterisation of a 2 W DUT. From the figure, it can be seen that there is also attenuation before the signals are sampled by the oscilloscope. The power budget not only protects the DUT, it also useful for protecting the measurement system.

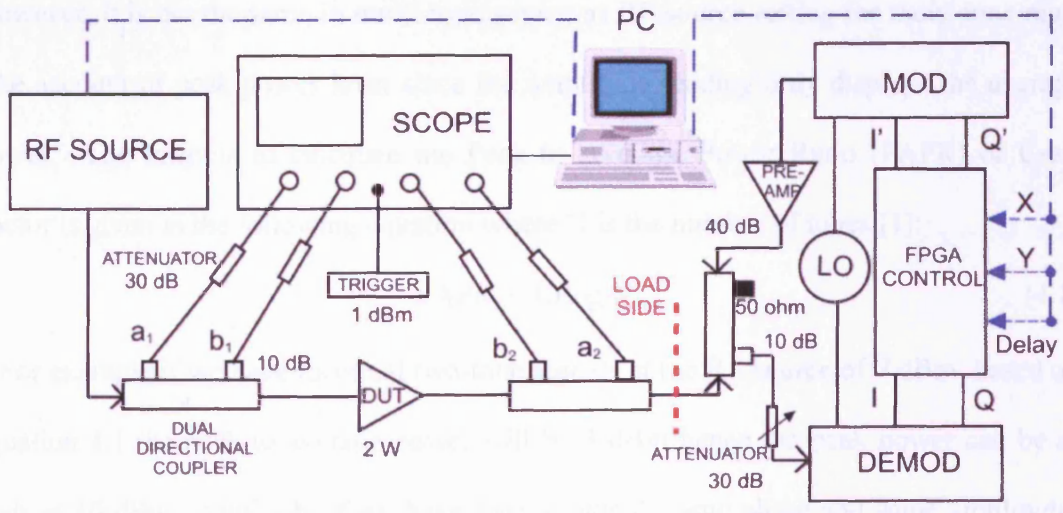

Figure 4.2: Power budget for multi-tone active envelope load-pull measurement system

i. RF source

Multi-tone panel option has to be ON for generating multi-tone signals. Since the multi-tone measurement software only support odd number of tones, thus for even

number of tones the RF source need to be configured accordingly. For example if we want 2 MHz two-tone, the entry for number of tones need to be configured in the measurement system is 3 tones with tone spacing of 1 MHz. After the RF source has been configured, the even middle tone (carrier) is suppressed. Effectively now we have 2 MHz two-tone. The general formula of configuring multi-tone can be summarized as follows. If we want N even number of tones with modulation frequency of k MHz we need to set up 2N-1 tone with tone spacing of k/2 MHz. Then after the RF source has been configured, the even tones are suppressed to give the required N (even) number of tones with k MHz spacing.

RF source CW setting for measurement system is straight-forward because whatever power level generated by the source is directly displayed in the amplitude reading. However, it is not the same in multi-tone source as RF source setting for multi-tone must take account of peak power level since the amplitude reading only displays the average power. The formula to calculate the Peak to Average Power Ratio (PAPR) or Crest Factor is given in the following equation where N is the number of tones [1]:

$$\text{PAPR} = 10\log N \tag{4.1}$$

For example if we have identical two-tone signals at the RF source of 7 dBm, based on equation 4.1 the peak to average power will be 3 dBm hence the peak power can be as high as 10 dBm. Similarly if we have four identical (same phase and same amplitude) four-tone signal at the RF source of 7 dBm, based on equation 4.1 the peak to average power will be 6 dBm hence the peak power can be as high as 13 dBm. If we have a device of maximum input power of 10 dBm, giving an identical four-tone signals at

amplitude reading (average) of 7 dBm can damage the DUT. Note that for random or pseudo random multi-sine signal for emulating CDMA signal the calculation of peak power will be different since the amplitude and phase of individual tones is different. Correctly designed multi-sine CDMA signals should not have more than 8 dB peak-to-average power.

ii. Directional Coupler

The directional coupler used is from Krytar with 10 dB coupling. It has SMA female connector with maximum insertion loss of 0.9 dB. Thus the demodulator without attenuation should receive about 10 dB less power than the RF b_2 wave.

iii. Demodulator

The I/Q demodulator is a cheap off-the-shelf component from Analog Device. The demodulator was used with the prototyping board that is available from the Analog Device website. It has single ended output that is suitable to be used with the FPGA board. This is possible because there are baluns at the differential outputs. These prevent the DC drift from disturbing the active envelope load-pull. Since the FPGA already has baluns at the ADCs and DACs, the drift would have been prevented in the first place.

In order to set up the demodulator properly the DC (5V) supply needs to be turned on, followed by the local oscillator (LO) and finally RF. To power down the demodulator, the sequence is reversed. Failure in following the sequence can damage the demodulator. Both the LO and RF maximum input limit is 0 dBm. Precautions need to be taken when doing multi-tone measurement since the amplitude displays on the spectrum analyzer do not give the actual peak power as mentioned in the RF source section.

iv. Modulator

The I/Q modulator is the built-in I/Q modulator inside Agilent Programmable Signal Generator (PSG). The active envelope load-pull uses the PSG as modulator by providing the baseband I/Q to the front panel of the PSG. To ensure that the resulting RF signal is from the I/Q generated from the digital controller not the PSG itself, PSG panel options are configured as shown in Table 4.2:

Table 4.2: PSG Modulator panel options configuration

Panel Options	**Configuration**
Multi-tone	OFF
I/Q	ON
Automatic Level Control (ALC)	OFF

The amplitude reading is left at the default 0 dBm. The I/Q panel graphic should display the diagram shown in Figure 4.3 when it is configured correctly.

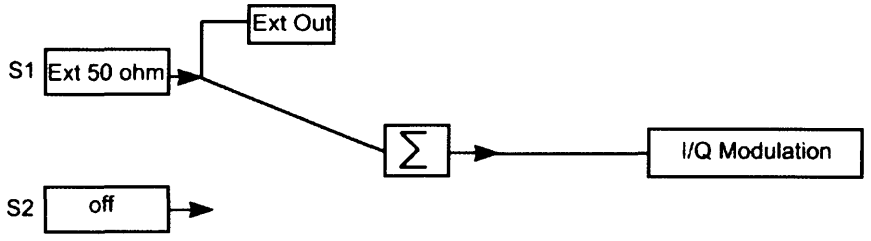

Figure 4.3: I/Q panel diagram displaying the external I/Q input

v. Local Oscillator (LO)

The LO is connected to both demodulator and modulator. If they are using different LO there may be a small phase drift. This is a common problem in open-loop active load-pull systems. This is due to the fact that the LO is in the GHz frequency range and the synchronisation for open active load-pull systems normally use the 10 MHz

synchronisation ports that are available in RF instruments. The mismatch frequency scaling of 100 between the synchronisation and the operating frequency can cause significant drift if the system is left running for considerable amount of time, i.e. overnight. Using the same LO for demodulator and modulator to ensure the same exact frequency in GHz range can mitigate the drift problem considerably.

vi. Oscilloscope

The high frequency digital sampling oscilloscope (DSO) is used as the time domain measurement tool. Modern high speed sampling oscilloscopes are well suited for precise measurement of microwave waveforms, modulated signals and non-linear phenomena [2]. The multi-tone measurement system uses a Tektronix high frequency digital sampling oscilloscope. This oscilloscope utilises modular samplers that can support up to tens of GHz signal frequencies with maximum input of 2.5V p-p or about 10 dBm. There are 30 dB attenuators between the directional coupler and the oscilloscope to protect the expensive samplers and the oscilloscope. The transformation to the frequency domain representations of the measured data can be performed in the host PC for measuring amplitude and phases of the components of a modulated RF/microwave signal.

vii. FPGA board

The operation of FPGA board for digital control has been described in Chapter 3. It can support input signal of 2 Vp-p or about 10 dBm. The power it can support is quite high but it is limited by the signal provided by the demodulator output. The positive feature is that since the modulator power level specification is quite high compared to demodulator, the digital controller can perform amplification in the digital domain to some extent. This functionality can be exercised by the scaler module block.

viii. Trigger

There are two trigger ports available for the oscilloscope, Trigger Prescale Input (2 – 12.5 GHz of maximum input 2.5 Vp-p) and Trigger Direct Input (DC – 3GHz of maximum input 1.5 Vp-p). Multi-tone measurement system uses the lower frequency Trigger Direct Input. The trigger signal is provided by the Arbitrary Waveform Generator (AWG). The setting is a rectangular wave, 500 mV p-p and 5 MHz. Through extensive testing it was found that a maximum clock frequency of 5 MHz should be used to ensure the sampling frequency remains constant throughout the measurement [3].

4.3 Delay Compensation

Any load-pull system, passive or active has group delay that causes the load for wideband signals to vary. It is impossible to compensate the delay inside passive load-pull system because by definition passive system does not inject external signal. Theoretically it is possible for active load-pull system to compensate for the delay. It is easier to compensate the delay in active envelope load-pull system because the control is performed at the lower baseband I/Q frequency regardless of the operating frequency.

Figure 4.7 represents the envelope of modulated signal with the following delay properties:

τ = group delay

Δ = delay compensation

T = repetition rate

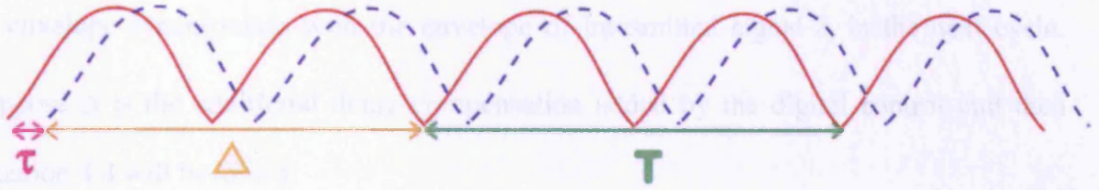

Figure 4.4: Measured Γ before delay compensation

From equation 2.11:

$$I'(t) + jQ'(t) = \Gamma[I(t) + jQ(t)] \tag{4.2}$$

where I'(t)+jQ'(t) and I(t)+jQ(t) represent the baseband components of the a_2 and b_2 signals respectively. The group delay τ in the loop modifies the envelope expression as follows:

$$I'(t) + jQ'(t) = \Gamma[I(t-\tau) + jQ(t-\tau)] \tag{4.3}$$

The effect of these group delay problems in the envelope feedback loop results in the load impedance becoming frequency dependent. Consider an n-tone signal of carrier frequency ω_c and tone spacing ω_m. From Equation 2.8 the resulting load impedance will be given as follows [7] :

$$\Gamma(\omega_c + n\omega_m) = (X + jY)e^{-jn\omega_m\tau} \tag{4.4}$$

where, n = ± 1, ± 2, ±3.... ±N

based on equation 4.4 the phase operator will cause phase spread in the load impedance at $(\omega_c - n\omega_m)$ and $(\omega_c + n\omega_m)$. This phase spread phenomenon makes the load impedances frequency dependent. Due to the group delay, the envelopes of transmitted and reflected signals are not synchronized. A feature of the sampling based system is that it uses repetitive signals, hence it is possible for reflected signal a_2 to be delayed further so that

its envelope synchronises with the envelope of transmitted signal b_2 in the next cycle. Suppose Δ is the additional delay compensation added by the digital control unit then equation 4.4 will becomes:

$$\Gamma(\omega_c + n\omega_m) = (X + jY)e^{-jn\omega_m(\tau+\Delta)} \tag{4.5}$$

where, n = ± 1, ± 2, ±3.... ±N

If the transmitted signal b_2 has repetition rate T then the compensated equation 4.3 will becomes:

$$I'(t) + jQ'(t) = \Gamma[I(t-\Delta-\tau) + jQ(t-\Delta-\tau)] \tag{4.6}$$

where $\Delta = T - \tau$

If Δ is set correctly then $T = \Delta + \tau$ therefore equation 4.6 is equivalent to equation 4.2, meaning that the delay is successfully compensated.

The delay compensation investigation of active envelope load-pull is made using a thru as the DUT. Thru measurement is performed using the same set up as Figure 4.1. The power levels however need to be modified accordingly in order to provide the correct power budget. The attenuator and the power amplifier have to be removed from Figure 4.2 to cater for the fact that there is no DUT amplification.

An RF power transistor measurement involving a suppressed carrier two-tone stimulus is a common approach to measuring and characterizing its linearity behaviour. In such measurement the output signal contains, in addition to the original two-tone stimulus, additional tone pairs corresponding to at least fifth order inter-modulation distortions processes. Hence, even in this case, the RF output is a multi-tone signal around the suppressed carrier covering at least five times the original modulation bandwidth.

It is important to note that this digital controller implementation is not DC coupled, because of the input A/D and output D/A baluns, hence it is limited to suppressed carrier stimulus investigations with modulation rates above 400 KHz. A suppressed carrier six-tone stimulus is therefore used to emulate both the increased signal complexity and bandwidth. It represents inter-modulation distortions effects that can be introduced by the power amplifier or transistor around the fundamentals or in-band frequency [4].

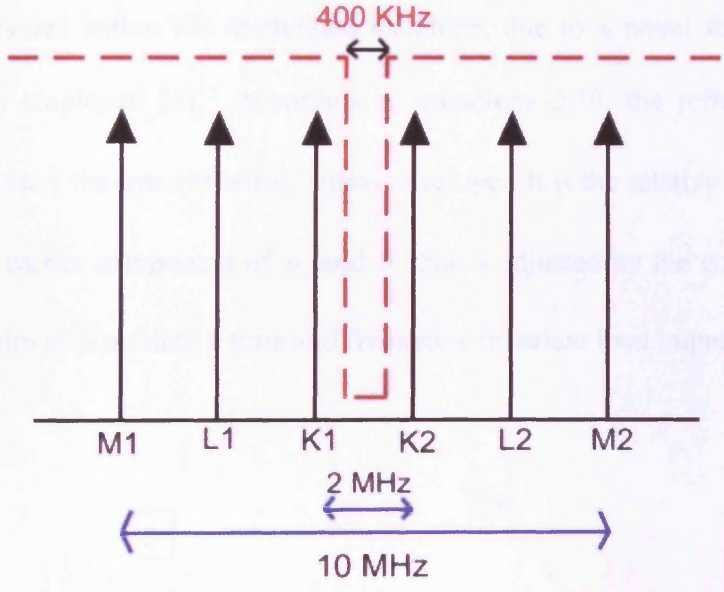

Figure 4.5: Six-tone stimulus signal, showing the spectral mask of digital controller

Figure 4.5 show six-tone stimulus signal used for the thru measurement. The suppressed carrier is at 900 MHz. The tones of K1 and K2 pair are emulating fundamentals of F1 and F2. Additional tones are necessary in order to emulate the effect inter-modulation in this thru measurement. In this particular investigation tones L1 and L2 pair emulating the IMD3s pair whereas tones M1 and M2 pair are emulating IMD5s pair. The modulation bandwidth is 2 MHz and the overall bandwidth including M1 and

M2 pair is 10 MHz, i.e. five times the modulation bandwidth. This addresses the bandwidth that would be necessary in a load-pull system to include the spectral re-growth from both third and fifth order distortion of a two-tone stimulus signal with a 2 MHz modulation bandwidth.

Figure 4.6 displays the measured RF reflected and transmitted waveforms, a_2 and b_2 before delay compensation. It should be noted that the waveforms have a reduced number of RF cycles within the modulated envelope, due to a novel folded sampling technique that is employed [3]. According to equations 2.10, the reflected a_2 signal envelope should track the transmitted b_2 signal envelope. It is the relative magnitude and phase of the RF carrier component of a_2 and b_2 that is adjusted by the control values X and Y, with the aim of providing a time and frequency invariant load impedance.

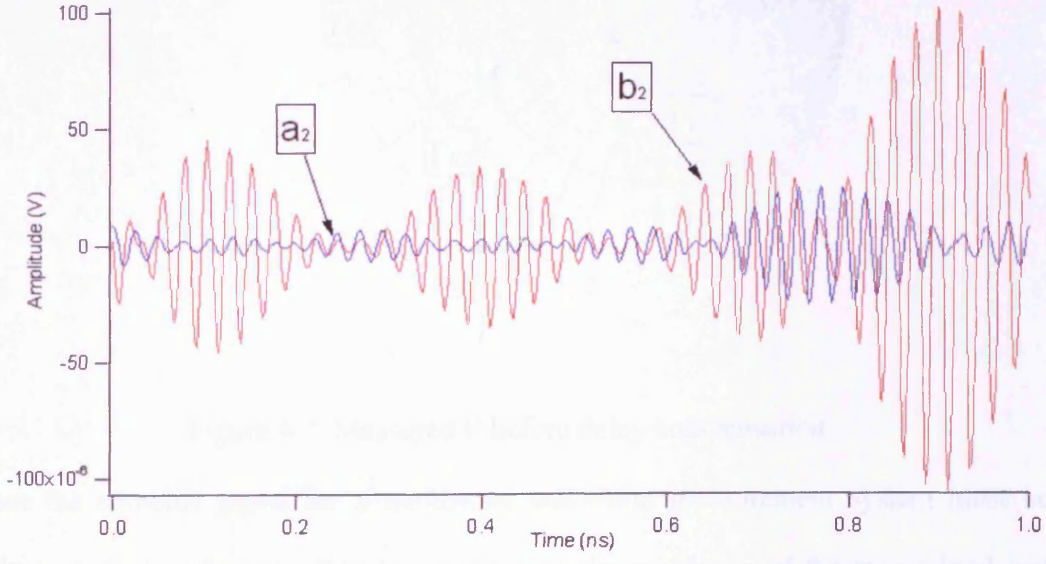

Figure 4.6: Measured waves for transmitted and reflected waves before delay compensation

The data in Figure 4.6 clearly indicates that the digital control unit is capable of operating with such a wide bandwidth envelope signal. Unfortunately, the complete feedback loop introduces an additional undesired delay to the envelope signal. As a consequence of this envelope delay the Γ presented to each of the tones is not constant, hence the resulting load-pull impedance varies significantly for each tone, as shown in Figure 4.7. Thus for the active envelope load-pull to function correctly this delay must be compensated in the digital control unit.

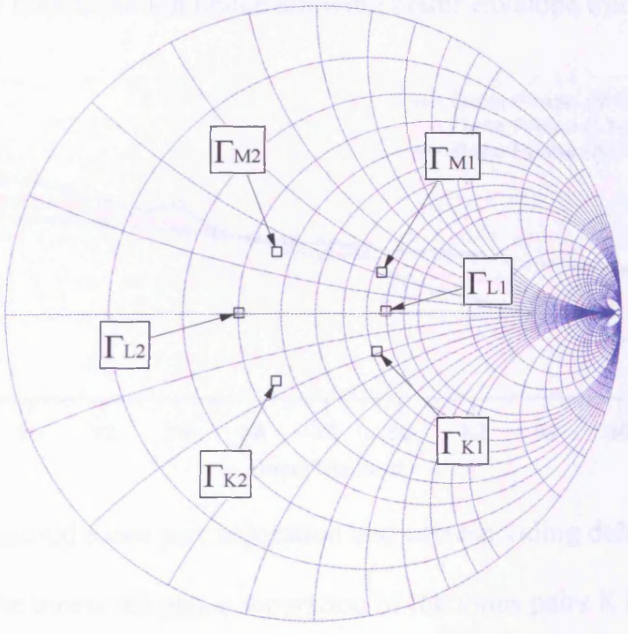

Figure 4.7: Measured Γ before delay compensation

Since the stimulus signal for a multi-tone waveform measurement system must be repetitive, it is therefore possible to synchronize the envelopes of the transmitted and reflected signals by increasing further the total loop delay until it becomes equal to the signal repetition period [5].

In the digital implementation this delay compensation is easy to achieve since the additional delay is simply realized inside the FPGA itself using a RAM based delay technique as described in Chapter 3. The delay is controlled by the same interface used to set the X and Y values. It also utilizes the in-system memory content editor (ISMCE) feature of the FPGA. An identical delay is applied for both I and Q channels in order to avoid I/Q imbalance. A unit element delay is equivalent to one clock cycle that is equivalent to 10 ns delay. Higher clock cycles for the FPGA will therefore provide better resolution for the delay compensation hence allowing better envelope tracking.

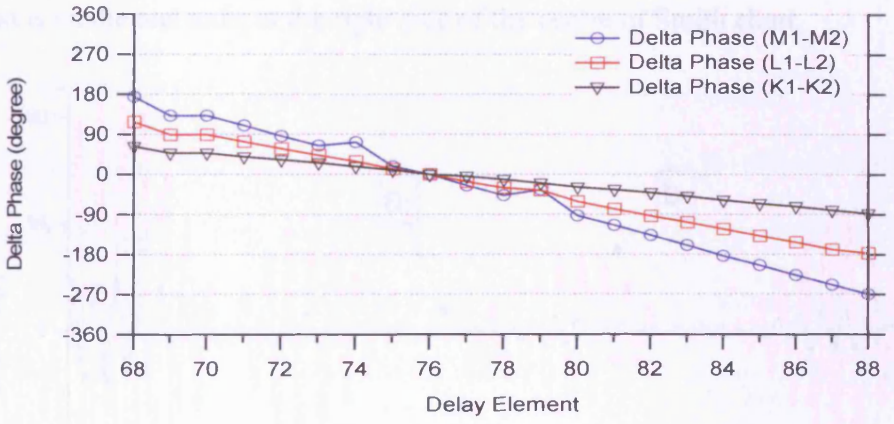

Figure 4.8: Measured tones pair separation and corresponding delay element

Figure 4.8 displays the measured phase separation of the tones pairs K1-K2, L1-L2 and M1-M3 as a function of the RAM based delay element. Ideally when the reflected wave is tracking the transmitted wave there should be zero phase separation between the two envelopes. The optimum delay compensation is found to be 76 unit or 760 ns with 10 ns for each unit delay. Since the control is applied to each channel of 1 MHz (modulation bandwidth of 2 MHz), the signal repetition rate is equals to 1 μs or 1000 ns. Comparing to Figure 4.4, if the delay compensation (Δ) is 760 ns and the repetition rate (T) is 1000

ns, it can be deduced that group delay τ is as follows:

$$\text{Group delay } (\tau) = 240 \text{ ns} + m(1000) \text{ ns} \quad (4.7)$$

where, m = 0, 1, 2, 3.... N

Figure 4.9 displays the measured modulated travelling waves achieved after introducing optimum delay compensation. Figure 4.9 exhibits the capability of digital control unit after compensation to ensure that envelopes of the transmitted and reflected RF signals now track. Note that the RF signals for a_2 and b_2 only phase aligned if it is in open or pseudo-open condition. In other words RF signal is only aligned if the load emulation is on the real axis, at the right side of the centre of Smith chart.

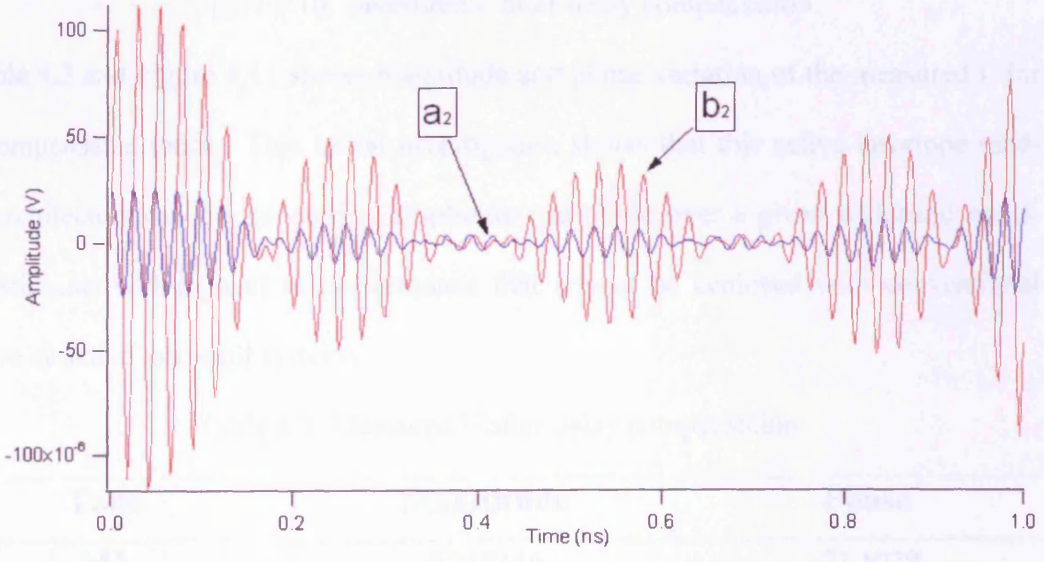

Figure 4.9: Measured waves for transmitted and reflected waves after delay compensation

Figure 4.10 displays the Γ achieved after introducing optimum delay compensation. It shows that the Γ for all six tones reside at almost the same location after the delay compensation, i.e. the desired carrier Γ at RF. This means this active load-pull architecture is capable of presenting constant Γ emulation over wide bandwidth.

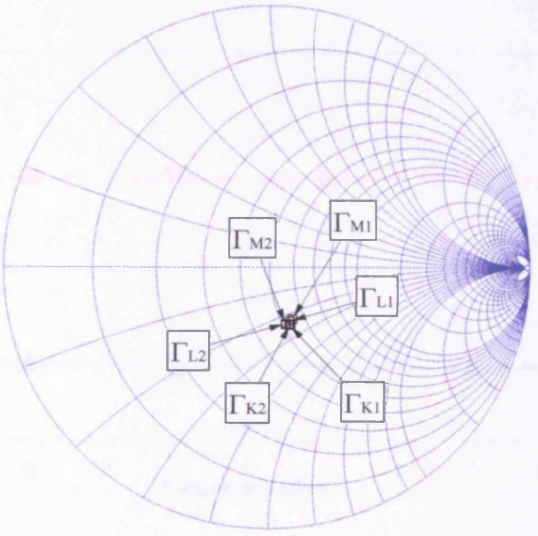

Figure 4.10: Measured Γ after delay compensation

Table 4.3 and Figure 4.11 shows magnitude and phase variation of the measured Γ for the compensated tones. This initial investigation shows that this active envelope load-pull architecture can tracks varying amplitude and phase over a given wideband multi-tone stimulus with a level of performance that cannot be achieved with conventional passive or active load-pull systems.

Table 4.3: Measured Γ after delay compensation

Tone	Magnitude	Phase
M1	0.218146	-71.1029
L1	0.220969	-69.5377
K1	0.234951	-69.0166
K2	0.232027	-73.8327
L2	0.225395	-65.9714
M2	0.229054	-74.2471

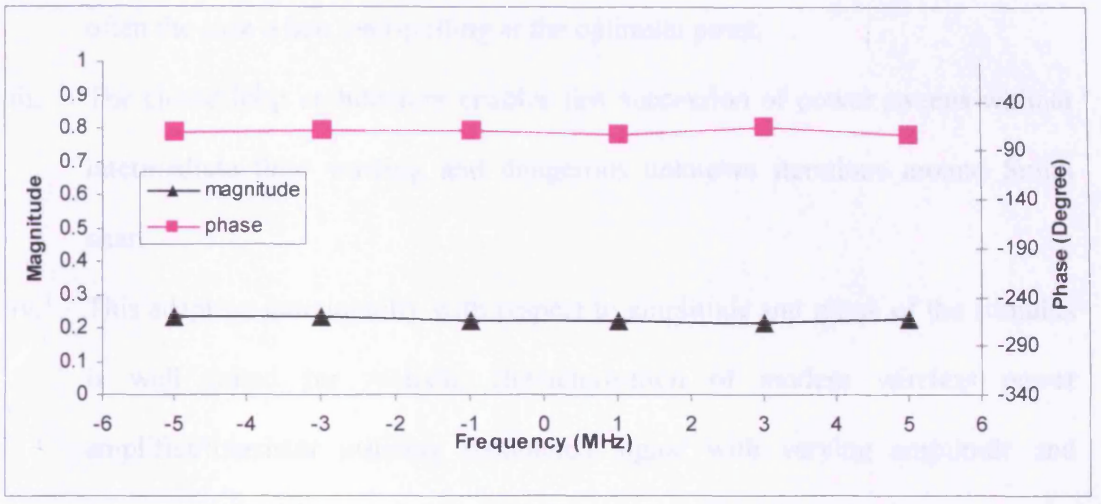

Figure 4.11: Measured Γ after delay compensation

4.4 Stimulus Adaptation Verification

According to equation 2.12, the active envelope load-pull is a closed-loop system. This means the reflected emulated a_2 to the output of the DUT is a function of the transmitted b_2 which is the output of the DUT itself. This closed-loop feature should make the active envelope load-pull stimulus independence. This is due to the fact that Γ is a ratio between a_2 and b_2 as given in equation 2.8. Hence any increase or decrease in transmitted b_2 signal would be 'reflected' in the a_2 signal resulting on the same value (magnitude and phase) of Γ.

The advantages of adaptive functionality resulting from the closed-loop architecture, compared to open-loop can be summarised as follows:

i. The closed-loop architecture enables the active envelope load-pull to set the load emulation instantaneously without iteration.

ii. Load emulation without iteration, mitigates DUT oscillation when working

close to instability region and beyond power transistor compression point as often the case when load-pulling at the optimum point.

iii. The closed-loop architecture enables fast succession of power sweeps without intermediate time wasting and dangerous unknown iterations around Smith chart.

iv. This adaptive functionality with respect to amplitude and phase of the stimulus is well suited for realistic characterisation of modern wireless power amplifier/transistor utilising modulated signal with varying amplitude and phase.

v. Advance modern power amplifier architecture with dynamic biasing, for example envelope tracking, can be characterised easily with the help of the adaptive functionality.

In order to illustrate this functionality in a real measurement environment, the stimulus is tested on 1W Mini Circuit power amplifier available off-the-shelf. The two-tone stimulus used in this investigation has operating carrier frequency of 1850 MHz and the modulation frequency of 2 MHz. The overall bandwidth when IMD5 is taken into consideration is 10 MHz, which is five times the modulation bandwidth. The delay is compensated up to IMD5 when the power amplifier was driven hard into compression as shown in Figure 4.12. Note that the load-pull grid points shown in Figure 4.12 are used as a guide during verification. The stimulus adaptation verification is performed by varying the phase and the amplitude of the two-tone stimulus.

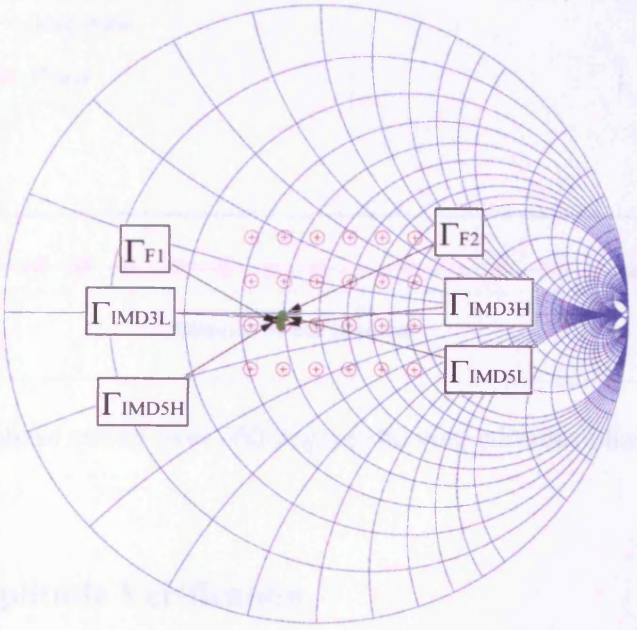

Figure 4.12: Measured Γ for two-tone stimulus when the power amplifier was driven hard into compression.

4.4.1 Adaptive Phase Verification

Conventional wireless standards such as the popular GSM standard uses Gaussian filtered Minimum Shift Keying (GMSK) modulation that only varies the phase of the signal but not the amplitude. Unlike open active load-pull, the closed-loop active load-pull should be able to track the varying phase by providing constant load emulation. Figure 4.13 shows the constant load emulation for swept phase of stimulus over 360 degree. Note that the Γ value is taken for the lower fundamental f1 tone (Γ_{f1}) only.

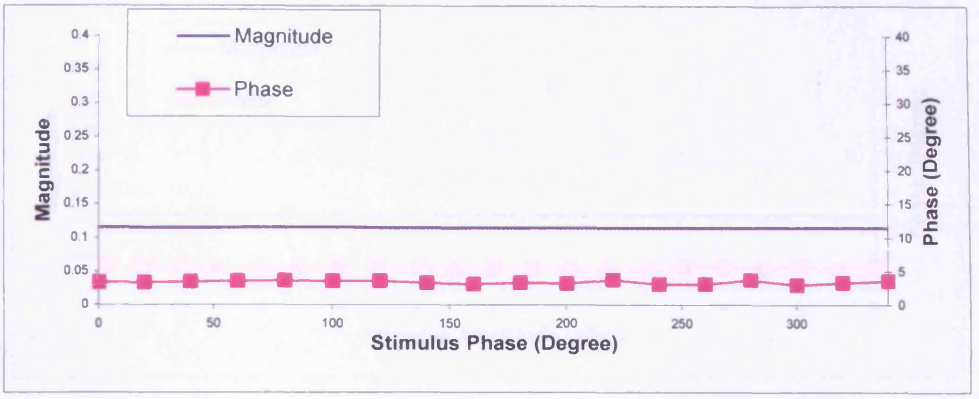

Figure 4.13: Stimulus phase sweep over 360 degree showing stimulus phase independent load emulation for Γ_{f1}

4.4.2 Adaptive Amplitude Verification

Modern wireless standards such as mobile WIMAX uses variety of modulations that are predominantly involve varying the amplitude and phase of the signal. One such modulation is Quadrature Amplitude Modulation (QAM). The active envelope load-pull is able to track the amplitude and phase variation. In the previous section we have already swept the phase. In this section we have swept amplitude of the stimulus in 20 dB range. The result is shown in Figure 4.14. Note that the Γ value is taken for the lower fundamental f1 (Γ_{f1}) tone only. From this result and the result from previous section it can be concluded that the active envelope-load pull can provide stimulus independent load emulation. It means that the active envelope load-pull system can support device characterisation for modern wireless standards that employs varying phase and amplitude. Coupled with the fact that the load-pull system use generic I/Q demodulator, hence it can handle all of current and future wireless standards provided it can support the required dynamic range and bandwidth.

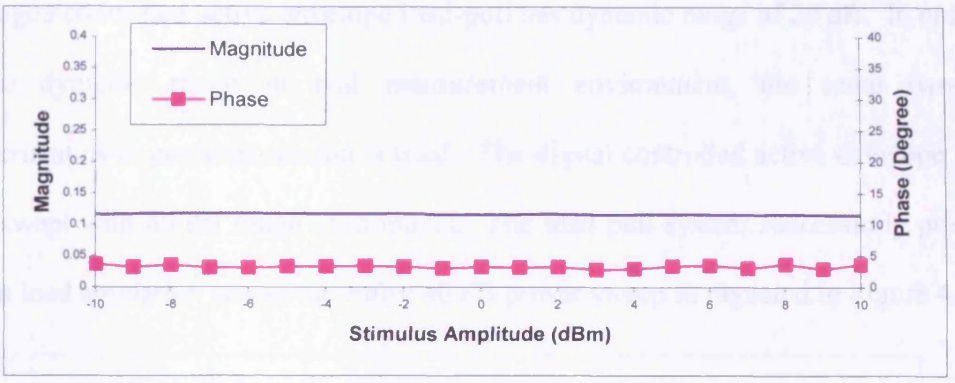

Figure 4.14: Stimulus power sweep over 20 dB range showing stimulus amplitude independent load emulation for Γ_{f1}

4.5 System Capability Investigations

It is important to investigate the capability of the active envelope load-pull. The main capabilities include dynamic range and bandwidth. This is due to modern wireless standards having modulation techniques with increasing spectral efficiency and bandwidth. Hence in order to provide realistic stimulus the dynamic range and bandwidth need to be quantified. In addition, the baluns limit the operating frequency of the digital controller. These investigations were performed using the same set up as the previous section using 1W Mini Circuit power amplifier as the DUT.

4.5.1 Dynamic Range Investigation

Dynamic range is important for any RF measurement system. The simple rule is that the higher dynamic range, the better. For load-pull system dynamic range requirement is not as high as normal measurement system like VNA. The reason is that load-pull is used primarily for strong non-linearity investigation and the non-linear effect of the IMD normally only significantly take effect beginning at 30 dBc.

Analogue controlled active envelope load-pull has dynamic range of 20 dB. In order to test the dynamic range in real measurement environment, the same two-tone measurement as in previous section is used. The digital controlled active envelope load-pull is swept with 40 dB range of stimulus. The load-pull system successfully presents constant load emulation across the entire 40 dB power sweep as depicted in Figure 4.15.

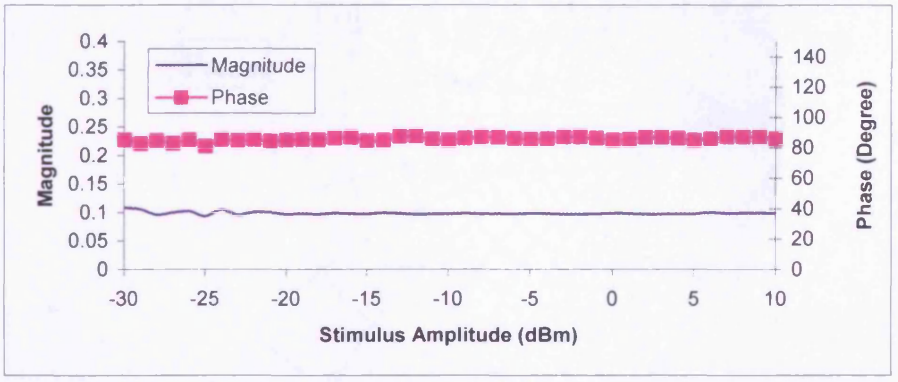

Figure 4.15: Stimulus power sweep over 40 dB range showing stimulus amplitude independent load emulation

There are two ways of determining the dynamic range of the active envelope load-pull system from the measurement of the power amplifier. In the first technique, two extreme values of power sweep, the highest and the lowest stimulus amplitude are used to determine the dynamic range. The dynamic range is calculated from the different between the highest and the lowest amplitude of the output power of the fundamentals. Figure 4.16 shows the Γ distribution for the lowest stimulus amplitude power at -30 dBm. The Γ for the lower and higher fundamental tones are both giving constant load emulation. The Γ for IMD3 and IMD5 pairs, however, are not giving constant load emulation. This is due to the fact that the power amplifier is in linear operating region and their IMDs values are very low and beyond the dynamic range of the system.

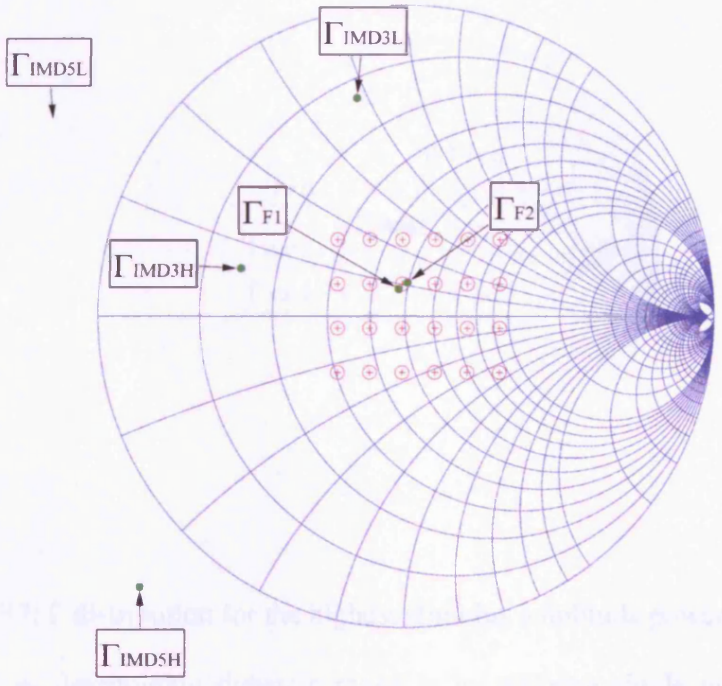

Figure 4.16: Γ distribution for the lowest stimulus amplitude power at -30 dBm

Figure 4.17 shows the Γ distribution for the higher stimulus amplitude power at 10 dBm. The active envelope load-pull system successfully presents constant load emulation for all of the in-band tones (fundamentals, IMD3 and IMD5). This is possible since the amplifier is driven well beyond the compression point. At the top of the dynamic range sweep with amplitude stimulus of 10 dBm, the lower fundamental has output power of 15 dBm whereas at the bottom of the dynamic range with amplitude stimulus of -30 dBm, the lower fundamental has output power of -17 dBm. Hence it can be concluded that the active envelope load-pull has actual dynamic range of 32 dB. The 40 dB range stimulus sweep does not reflect the actual dynamic range since at the higher

amplitude stimulus range the power amplifier actually went into compression with the output becoming saturated beyond the compression point.

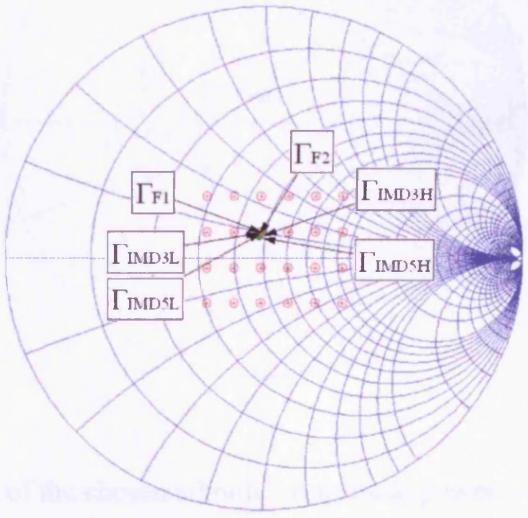

Figure 4.17: Γ distribution for the highest stimulus amplitude power at 10 dBm

Another way of determining dynamic range is by utilising single amplitude of the stimulus power. The power sweep value is chosen from the minimum stimulus amplitude that has output with fundamentals and IMD3s at the desired load emulation point as shown in Figure 4.18. The dynamic range is calculated from the difference between the amplitude of the lower fundamental tone and the lower third order of inter-modulation, IMD3L. The dynamic range calculated from this technique is about 37 dB. This technique can be easily understood by referring to the output power spectrum as shown in Figure 4.19.

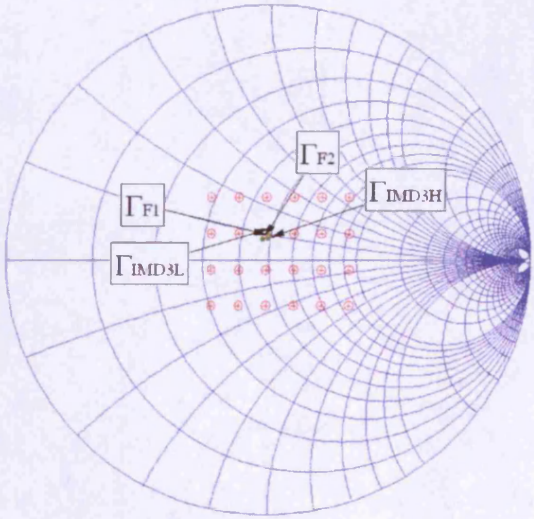

Figure 4.18: Γ distribution of the chosen stimulus amplitude power with constant load emulation up to IMD3 at -3 dBm stimulus

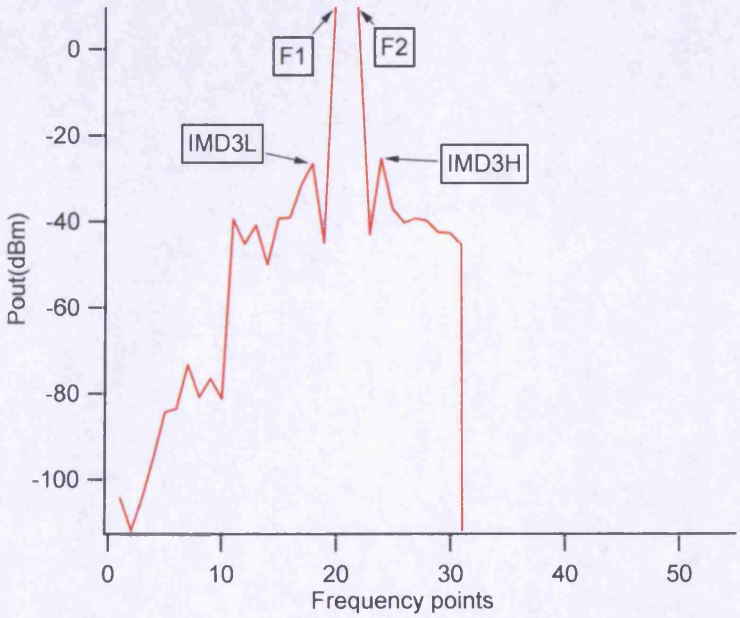

Figure 4.19: The output power spectrum indicating the dynamic range between fundamentals and IMD3 at stimulus amplitude of -3dBm

To further verify the validity of the second technique the dynamic range between the fundamentals and IMD5 can also be calculated. Quite similar with the first approach, single input stimulus amplitude is chosen from the minimum value that has the output of the fundamentals, IMD3s and IMD5s are all at the same load-pull point, i.e. load emulation is constant up to IMD5s as shown in Figure 4.20.

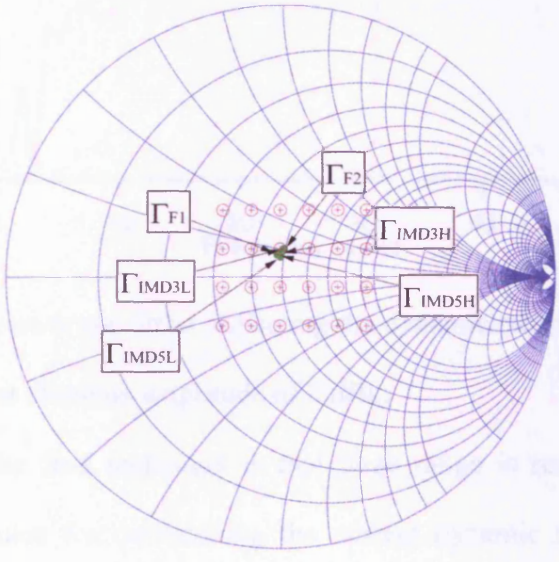

Figure 4.20: Γ distribution of the chosen stimulus amplitude power with constant load emulation up to IMD5 at 0 dBm

The dynamic range is calculated from the difference between the amplitude of the lower fundamental tone and the lower fifth order of inter-modulation, IMD5L. The dynamic range calculated from this technique is also about 37 dB i.e. identical to the dynamic range found in the first approach of the second technique. The output spectrum is depicted in Figure 4.21.

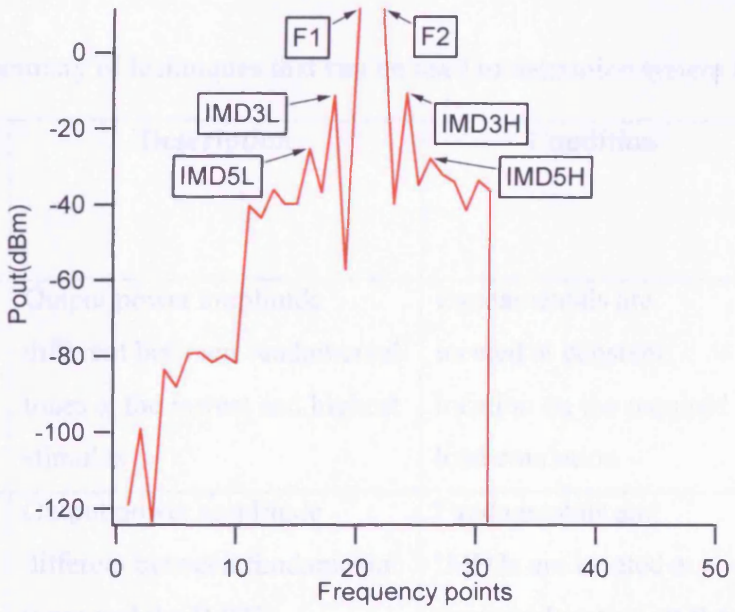

Figure 4.21: The output power spectrum indicating the dynamic range between fundamentals and IMD5 at stimulus amplitude of 0 dBm

The disadvantage of the first technique is that huge range is required between the highest and lowest stimulus for determining the correct dynamic range. The 40 dB dynamic range of the stimulus between highest and the lowest stimulus, however, is still not enough to calculate the correct dynamic range between the two extreme fundamentals. The second technique however is better since only one amplitude stimulus is needed and it can be verified further with another suitable amplitude stimulus. In reality, however, several power sweeps are still required in order to determine the stimulus amplitude where the load emulation is constant for fundamentals, IMD3 and IMD5. The second approach obviously can be further extended to IMD7 for even further verification. Table 4.4 summarised both of the techniques used to determine the dynamic range for the active envelope load-pull system.

Table 4.4: Summary of techniques that can be used to determine system dynamic range

Technique	Description	Condition	Calculated Dynamic Range/dB
1st technique	Output power amplitude different between fundamental tones at the lowest and highest stimulus	Fundamentals are located at constant location on the required load emulation	32
2nd technique (1st approach)	Output power amplitude different between fundamental tones and the IMD3s	Fundamentals and IMD3s are located at constant location on the required load emulation	37
2nd technique (2nd approach)	Output power amplitude different between fundamental tones and the IMD5s	Fundamentals, IMD3s and IMD5s are located at constant location on the required load emulation	37

4.5.2 Bandwidth Investigation

Bandwidth is very important for multi-tone measurement system. The simple rule is that the higher bandwidth, the better. The recent trend, however, has increased the bandwidth requirement even further because of the higher modulation bandwidth requirement and higher spectrum utilisation or spectral efficiency, hence power amplifiers must be more linear. Both LTE and WIMAX can support up to 20 MHz bandwidth even though lower modulation bandwidth is also supported.

As shown in Figure 2.5, there are three main components in large signal time domain measurement system namely signal generator, oscilloscope and load-pull. The measurement system uses high specification signal generator (ESG) for the multi-tone stimulus generation and high frequency oscilloscope for capturing the measurement data. The oscilloscope has the highest bandwidth, followed by the ESG and load-pull has the least bandwidth. For linear DUT measurement, the load-pull system has to support at least equivalent bandwidth with the ESG while for non-linear measurement load-pull system has to support more bandwidth than the bandwidth of the ESG. Currently the load-pull system cannot even keep up with bandwidth of the stimulus that can be generated by the ESG. The matter is made worst by the fact that any non-linear system will produce a distorted a signal with at least five times the stimulus bandwidth. Hence five times bandwidth is required if up to the fifth inter-modulation distortions are to be considered. If higher inter-modulations are to be taken into account, the effective bandwidth requirement can be very large for measurement of modern wireless standards.

The existing analogue controlled active envelope load-pull has bandwidth of less than 1 MHz, thus it will struggle to even support inter-modulation distortions up to IMD5 even for the existing GSM wireless standard. Hence it has a long way from fulfilling the requirement of modern wireless standard. The digital controlled active envelope load-pull controlled is developed primarily to increase the bandwidth capability of the load-pull system so that it can provide load-pull measurement with more realistic characterisation stimulus.

In order to test the bandwidth of the active envelope load-pull in real measurement environment, the same two-tone measurement as in previous section is used. There are

two ways of determining the operating bandwidth of the active envelope load-pull system from the measurement of the power amplifier. In the first technique, the bandwidth is determined using the dynamic range established in the previous section. The premise is that within the measurement system dynamic range the Γ will be held constant over the bandwidth. The load-pull system successfully presents constant load emulation for modulation bandwidth of 4 MHz as depicted in Figure 4.22. Essentially, 4 MHz modulation bandwidth corresponds to overall bandwidth of 20 MHz up to IMD5. Figure 4.23 shows a more details representation of the inter-modulation. The IMD7 which equivalent to 28 MHz overall has a Γ deviates from the intended load emulation point although it is only at 36 dBc as shown in Figure 4.24. This 36 dBc range should be still supported by the digital control that has dynamic range of at least 37 dB as provided from the previous section. The deviation of the IMD7 from the intended load emulation point, therefore, is solely due to the fact that the digital controller does not provide flat response for 28 MHz bandwidth.

Mobile WIMAX or 802.16e wireless standard can support modulation bandwidth from 1.25 MHz to 20 MHz [6]. For 20 MHz modulation bandwidth, catering for fifth inter-modulation distortions (IMD5) requires 100 MHz bandwidth capability. Hence the active envelope load-pull can support measurement of realistic bandwidth stimulus for mobile WIMAX at the lower modulation bandwidth operation including their IMD5 inter-modulation distortions.

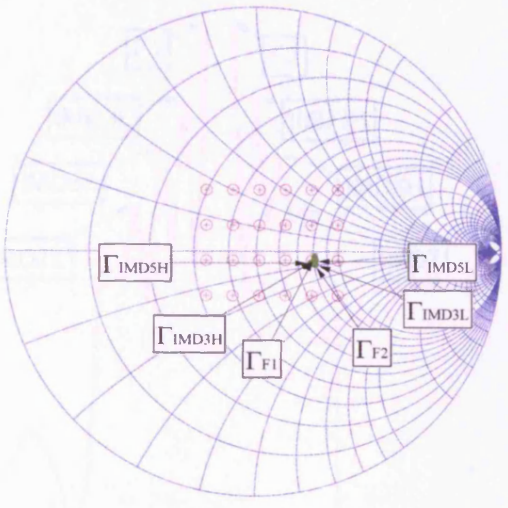

Figure 4.22: Constant load emulation at 4 MHz modulation bandwidth up to IMD5 or overall bandwidth of 20 MHz at 10 dBm

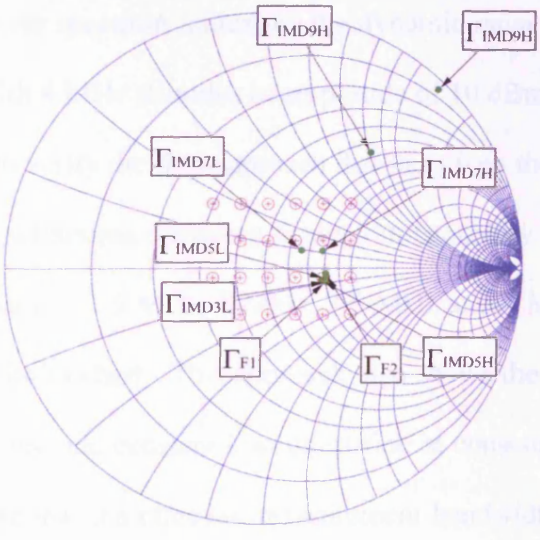

Figure 4.23: Constant load emulation at 4 MHz modulation bandwidth up to IMD9 or overall bandwidth of 36 MHz at 10 dBm

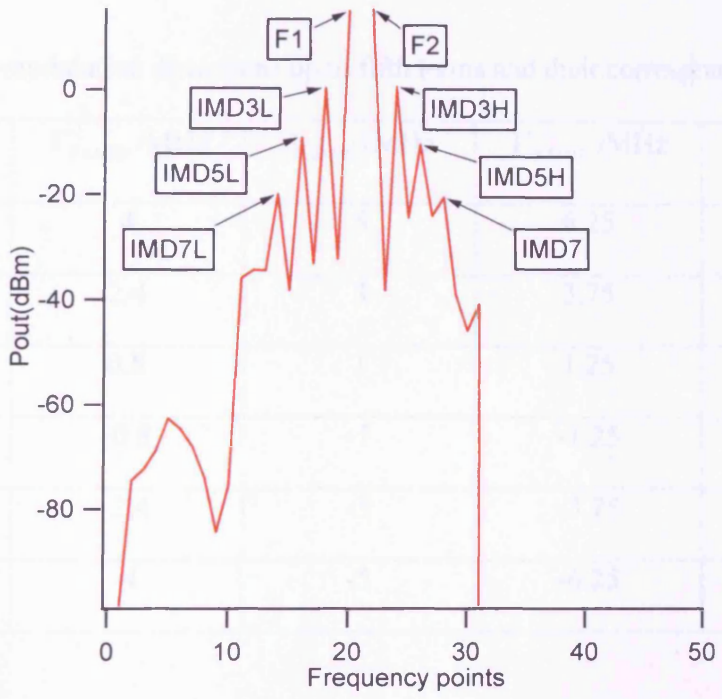

Figure 4.24: The output power spectrum indicating the dynamic range between fundamentals and IMD7 with 4 MHz stimulus at amplitude of 10 dBm

The second approach is to verify the first approach that has given the 20 MHz operating bandwidth. This approach scrutinizes operating bandwidth capability for four modulation bandwidth measurements namely 1.6 MHz, 2 MHz, 2.5 MHz and 4 MHz for load-pull at one reference point on the Smith chart. This approach also shows the versatility of active envelope load-pull that can provide constant load emulation at constant point for different modulation frequency. Note that the effective measurement bandwidth (up to fifth inter-modulation distortions) for 1.6 Mhz bandwidth is 8 MHz, for 2 MHz is 10 MHz, for 2.5 MHz is 12.5 MHz and for 4 MHz is 20 MHz as shown in Table 4.5.

Table 4.5 : Inter-modulation distortions up to fifth terms and their corresponding bandwidth

	$\Gamma_{1.6MHz}$ /MHz	Γ_{2MHz} /MHz	$\Gamma_{2.5MHz}$ /MHz	Γ_{4MHz} /MHz
IMD5U	4	5	6.25	10
IMD3U	2.4	3	3.75	6
F2	0.8	1	1.25	2
F1	-0.8	-1	-1.25	-2
IMD3L	-2.4	-3	-3.75	-6
IMD5L	-4	-5	-6.25	-10

Figure 4.25 and Figure 4.26 shows the magnitude and phase of Γ, respectively, for four different stimuli bandwidth of 1.6 MHz, 2 MHz, 2.5 MH, 4 MHz at 10 dBm power level. Each bandwidth stimulus is two-tone but the resultant inter-modulations up to IMD5 are six tones. Hence overall there are twenty four tones on Figure 4.25 and 4.26. Complete Γ values including the referenced load-pull point is given inside appendix E.

The magnitude of the referenced load-pull point is 0.119. The difference from the average or bias from the referenced magnitude is 0.119 – 0.116 = 0.003. Based on the bias the amplitude accuracy is about 97.5%. The phase of the referenced load-pull point is 71.36°. The bias from the referenced phase is 72.64° – 71.36° = 1.28°. Based on the bias the phase accuracy is about 98.2%. The combined accuracy of magnitude and phase is about 97.9% or close to 98% accuracy for four different measured stimulus modulation bandwidths.

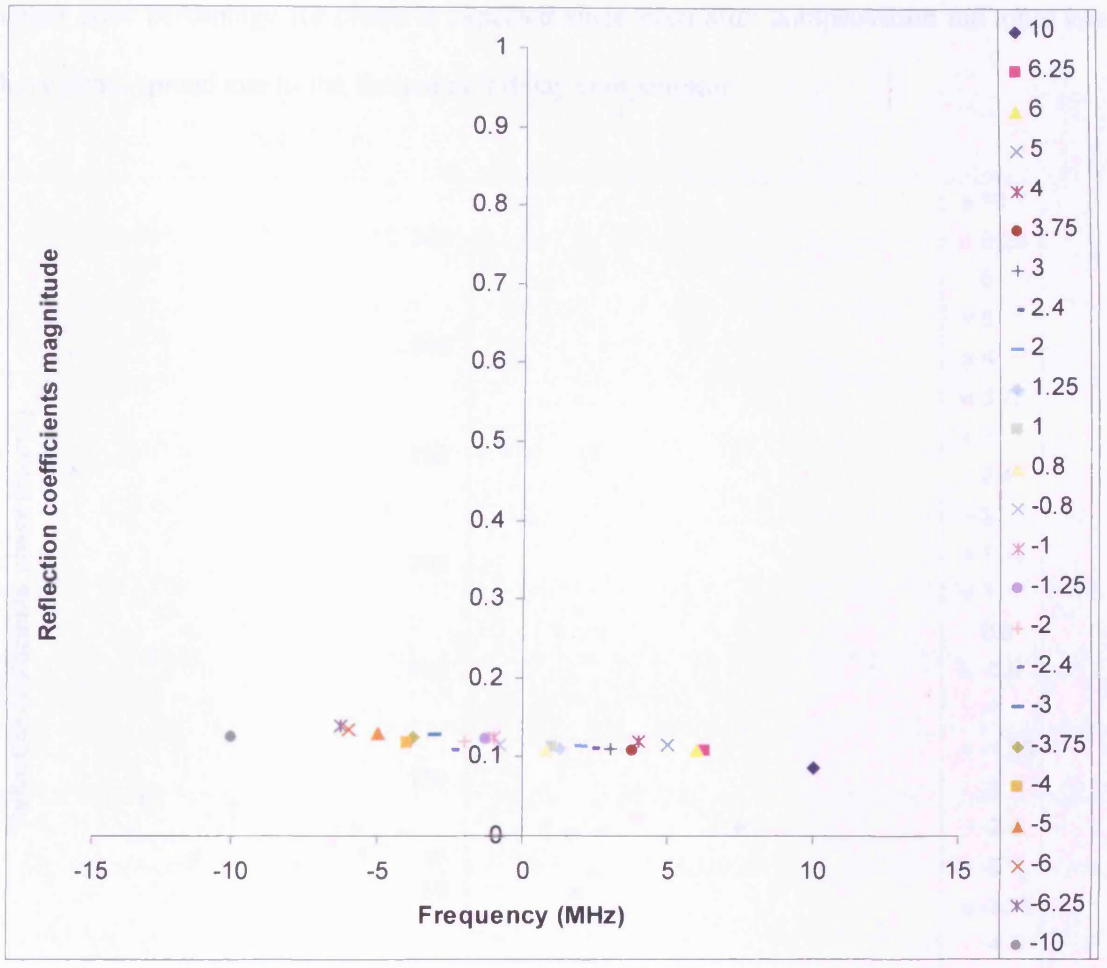

Figure 4.25: Magnitude of Γ for four different stimuli bandwidth of 1.6 MHz, 2 M Hz, 2.5 MH, 4 MHz at 10 dBm power

The referenced load-pull point is $0.119\angle 71.36°$. The calculated error deviation, with respect to the referenced load-pull point, of the magnitude is 0.0118 while the calculated error deviation of the phase is 8.07°. Hence the error deviation percentage for amplitude and phase are 9.9% and 11.3%, respectively. The amplitude and the phase errors are probably due to the impairments of the I/Q modulator and demodulator. The relatively

larger error percentage for phase is expected since even after compensation the tones can have phase spread due to the limited unit delay compensator.

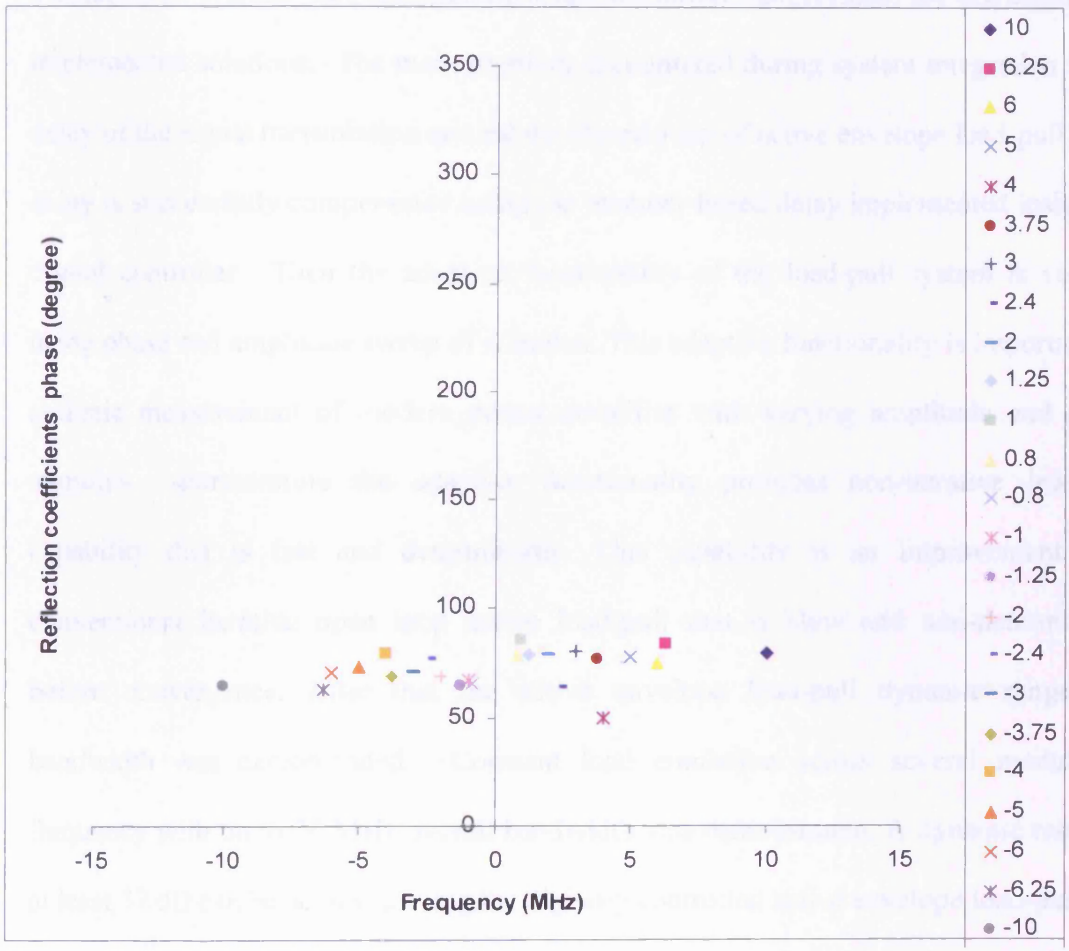

Figure 4.26: Phase of Γ for four different stimuli bandwidth of 1.6 MHz, 2 MHz, 2.5 MH, 4 MHz at 10 dBm power

4.6 Chapter Summary

In this chapter the developed digital controller is integrated into the multi-tone measurement system. The configurations and the power budget issues are discussed with implemented solutions. The main problem encountered during system integration is the delay of the signal transmission around the closed-loop of active envelope load-pull. The delay is successfully compensated using the memory based delay implemented inside the digital controller. Then the adaptive functionality of the load-pull system is verified using phase and amplitude sweep of stimulus. This adaptive functionality is important for realistic measurement of modern power amplifier with varying amplitude and phase stimulus. Furthermore the adaptive functionality provides non-iterative load-pull capability that is fast and deterministic. This capability is an improvement over conventional iterative open loop active load-pull that is slow and non-deterministic before convergence. After that the active envelope load-pull dynamic range and bandwidth was demonstrated. Constant load emulation across several modulation frequency with up to 20 MHz overall bandwidth was demonstrated. A dynamic range of at least 37 dB can be achieved using the digitally controlled active envelope load-pull.

4.7 References

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CHAPTER 5

APPLICATION OF WIDEBAND MULTI-TONE ACTIVE ENVELOPE LOAD-PULL

5.1 Load-Pull Perspective of Power Amplifier Measurement

Modulated non-linear power amplifier measurements are normally performed using passive load-pull and the measurement bandwidth is kept within the range of few MHz due to the delay variation introduced by passive architecture [1]. Modern load-pull measurements, however, requires the magnitude of reflection coefficient (Γ) to be more than unity, in order to compensate for the loss between the tuner and the coupler for advance power amplifier measurement hence the drives towards active load-pull. Active load-pull, however, cannot keep up with the number of tones due to the limitation of the popular open-loop architecture. Alternatively, less popular RF closed-loop active load-pulls do exist but the bandwidth is limited by the RF filter being used for avoiding oscillation and the delay spread of Γ is difficult to control since it is operating at high frequency.

Active envelope load-pull architecture shows promising functionalities and features that potentially can support realistic modern wireless standards that utilise linear modulations with varying amplitude and phase. Emerging fourth generations (4G)

wireless standards, for example LTE and Mobile WIMAX, has 20 MHz bandwidth that require at least 100 MHz load-pull bandwidth for including up to fifth inter-modulation distortions (IMD5). The main attraction of the newly developed active envelope load-pull is the capability of supporting higher bandwidth of tens of MHz and potentially hundreds of MHz if the digital hardware capabilities continue to improve. This high bandwidth capability is partly contributed by the ability to compensate for the delay spread or variation that becoming more significant as the bandwidth is increased beyond few MHz. Furthermore the ability to control the in-band impedances directly can provide useful insight into the effect that impedance variation of Γ can have on the characteristic of the power amplifier and transistor.

There are two DUTs, a power amplifier and a transistor, used to demonstrate the measurement application of the developed, digitally controlled active envelope load-pull. The first one is off-the-shelf packaged 1 W power amplifier from Mini-Circuit and another is a 2 W GaN HFET device from Cree. Both are biased in class A to minimise the effect of baseband and harmonics because the load-pull is only performed at in-band frequencies around the fundamentals. The 1 W power amplifier measurements is coaxial based whereas the 2 W GaN device is measured on-wafer. The measurement bench is similar to Figure 4.1 and the power budget needs to be adjusted according to the DUT power rating.

5.2 Power Amplifier Linearity Measurement

The power amplifier used in the measurement is a wide bandwidth (20 MHz to 40 GHz) packaged power amplifier from Mini-circuits with coaxial connections, model no. ZX60-

4016E. This power amplifier has rating of maximum power output of 17.4 dBm at 1 dB compression. The gain at carrier frequency 1850 MHz (the measurement frequency) is 18.2 dB.

Figure 5.1 displays very little variation of RF in-band reflection coefficients across 10 MHz bandwidth up to IMD5 at 8 dBm stimulus of 2 MHz bandwidth. Since this packaged power amplifier we would expect the optimum impedance point for maximum output power to be near the centre of the Smith chart.

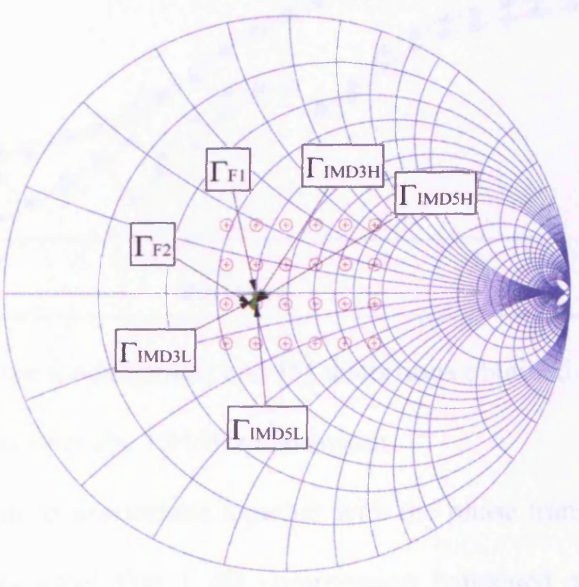


Figure 5.1: Measured variation of RF in-band reflection coefficients showing very little variation across 10 MHz bandwidth up to IMD5 at 8 dBm stimulus.

Figure 5.2 displays the power sweep AM-AM characteristic of the power amplifier showing amplitude of the fundamentals and IM distortions obtained under a fixed RF fundamental impedance, achieved over the 10 MHz bandwidth. The figure shows that the

fundamentals have very similar amplitude. The third order inter-modulation distortions (IMD3) is very symmetrical within the supported dynamic range. The asymmetry between fifth inter-modulation distortions (IMD5), however, is more noticeable within the supported dynamic range. The asymmetry in the inter-modulation distortions is due to memory effect [2].

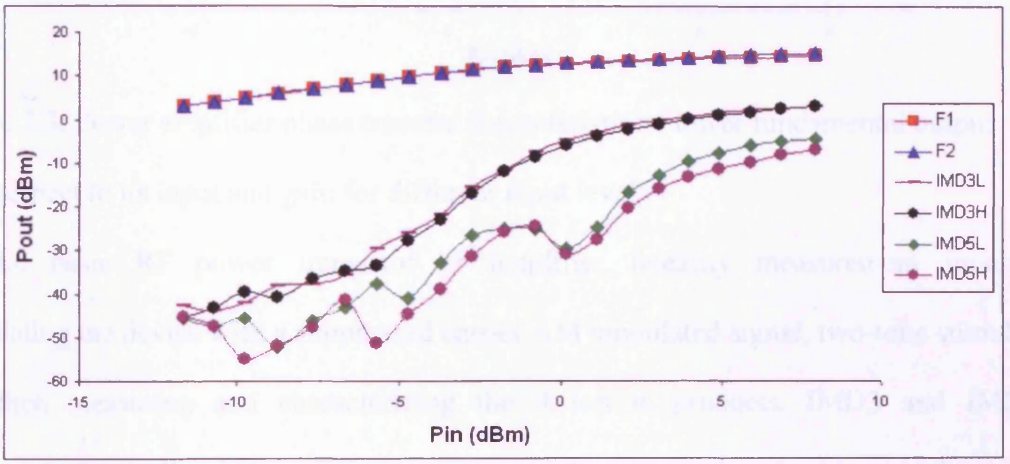


Figure 5.2: Amplitude of the fundamentals and IM distortions obtained under constant RF fundamental impedance over the 10 MHz bandwidth

Figure 5.3 shows the gain characteristic together with the phase transfer characteristic. The gain characteristic indicates that 1 dB compression happened at -1.8 dBm input power level. The phase transfer characteristic represents the lower fundamental output phase with respect to input phase. The phase response is quite linear over 20 dB dynamic range especially in the region before compression or the linear region.

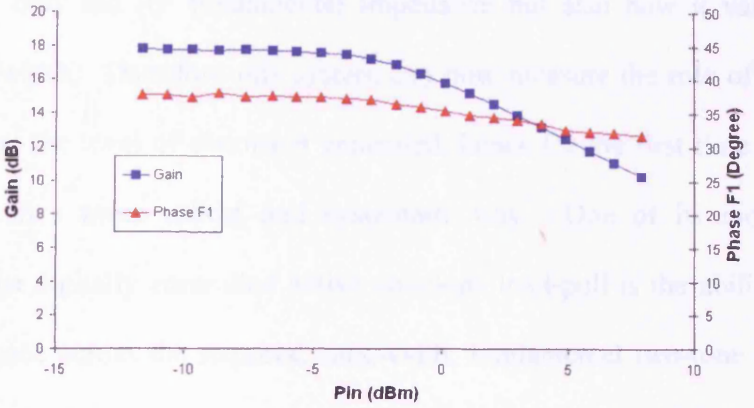


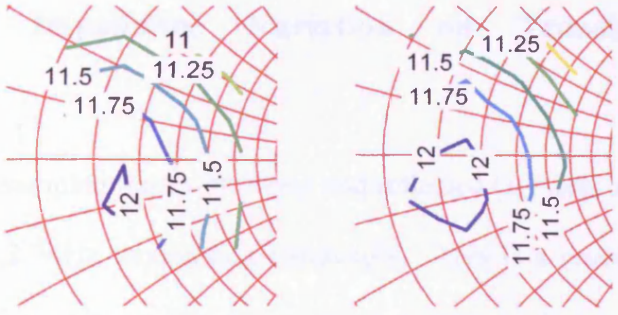
Figure 5.3: Power amplifier phase transfer characteristic of lower fundamental output with respect to its input and gain for different input levels

The basic RF power transistor or amplifier linearity measurement involves stimulating the device with a suppressed carrier AM modulated signal, two-tone stimulus, and then measuring and characterizing the distortion products, IMD3 and IMD5, generated. Typically, these measurements would then be combined with a passive load-pull system to investigate the variations of these distortions on the fundamental load-impedance; IMD3 linearity contours. Note, the output signal contains, in addition to the original two-tone stimulus, additional tone pairs corresponding to at least the fifth order inter-modulation distortion processes. Thus the RF output is actually a multi-tone signal with at least five times the original modulation bandwidth. Variation of fundamental RF impedance across the modulation bandwidth introduced by the passive load-pull system will also influence the distortion products. Hence, passive load-pull systems as the modulation bandwidth increases can corrupt and possibly generate misleading IMD3 and IMD5 linearity contours.

A key feature of the active envelope load-pull system developed in this work is that it

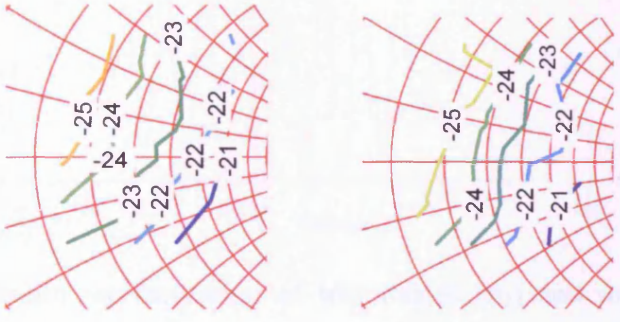
can control not only the RF fundamental impedance but also how it varies over the modulated bandwidth. Therefore this system can now measure the role of fundamental RF impedance on the level of distortion generated, hence for the first time allow this to be investigated in a more robust and systematic way. One of its most important capabilities of the digitally controlled active envelope load-pull is the ability to provide constant impedance across the required bandwidth, fundamental two-tone stimulus and the desired inter-modulation distortion bandwidth, as shown at a selected impedance point in Figure 5.1. Linearity contours which in this case are now dependent only on the variation of RF fundamental load impedance, hence no longer corrupted [3]. Results obtained are shown in Figure 5.4, 5.5 and 5.6. The plotted contours are for a constant input stimulus corresponding to that necessary to achieve a 1 dB gain compression point at the optimum impedance for maximum output power. Note that the contour values are absolute for fundamentals (dBm) but relative for the inter-modulations distortions (dBc).

This load-pull measurement demonstrated how, using the digitally controlled active envelope load-pull system, the linearity performance contours as a function of RF fundamental load impedance of a power amplifier can be evaluated robustly under wide bandwidth modulation. It provides a constant impedance environment across a wide modulation bandwidth including the inter-modulations although only the significant inter-modulations, IMD3s and IMD5s, are shown on the diagram. The possible corruption of the contours by impedance variation across the modulation bandwidth, present in established passive and active systems, is eliminated in this new system.



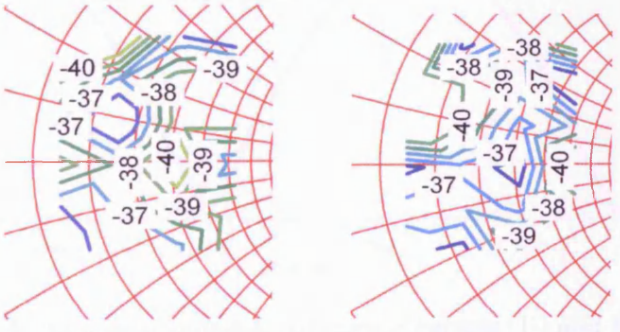
(a) (b)

Figure 5.4: Fundamental output power contours for lower (a) and higher (b) in dBm



(a) (b)

Figure 5.5: IMD3 contours for lower (a) and higher (b) in dBc



(a) (b)

Figure 5.6: IMD5 contours for lower (a) and higher (b) in dBc

5.3 Effect of Impedance Variation on Transistor Dynamic Characteristics

Figure 5.7 shows the sampled transmitted (b_2) and reflected (a_2) time domain RF signal at 2.1 GHz carrier and 2 MHz modulation bandwidth. This is a proof that the envelope load-pull can track the modulated signal precisely and dynamically.

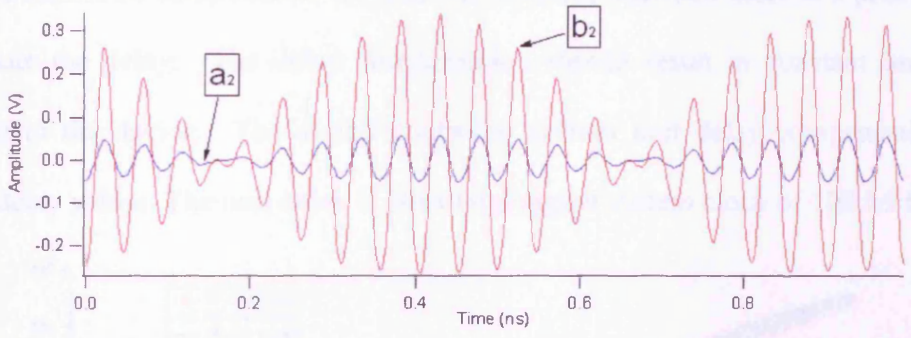


Figure 5.7: Time domain representation of transmitted (b_2) and reflected waves (a_2) indicating the successful tracking RF signal.

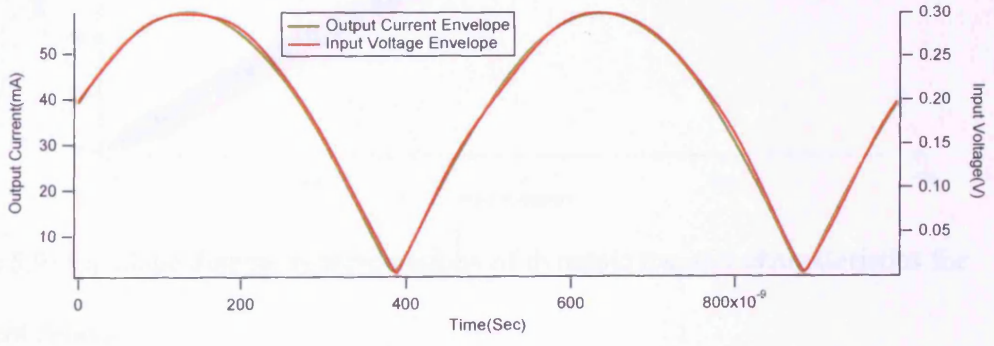


Figure 5.8: Envelope domain representation of output current (I_2) and Input voltage (V_1) indicating the successful tracking of the modulated envelop.

Figure 5.8 shows the envelope domain representation of output current and input voltage corresponding to transmitted (b_2) and reflected (a_1) waves. It demonstrates that the active envelope load-pull system can perfectly track the wideband modulated signal.

This also shows that the device has no memory since output current tracks input voltage. This may well be due to the fact that the load-pull system tracks and thus has no memory.

The in-band impedance, i.e. impedance of the fundamentals and the inter-modulation distortions product, in passive or active load-pull varies with frequency due to the delay in the measurement system. The problem is that in passive load-pull the impedance variations cannot be compensated for whereas in active load-pull there is a possibility to compensate the delay. The delay compensation should result in constant impedance presented to the device. The digital controller utilizes unit delay compensation with discrete delay values. The unit delay is 10ns for a digital system clock of 100 MHz.

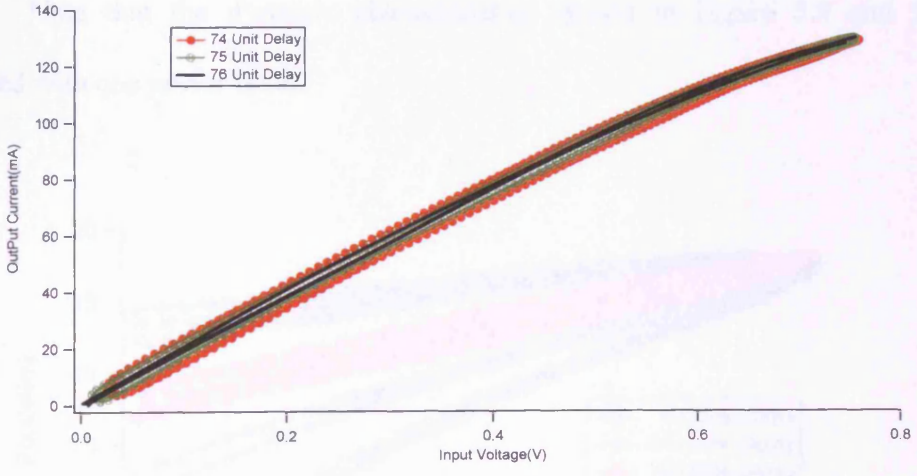


Figure 5.9: Envelope domain representations of dynamic transfer characteristics for different delays

Figure 5.9 shows the envelope domain representation of the dynamic transfer characteristics of the device for different delays. The loops are caused by the impedance variations across the in-band tones. The compensated optimum delay is 76 units where the response has the smallest loop. The response loop size increases as the unit delay

numbers are deviating from the compensated delay value of 76 units.

Even though the delay compensation does minimise the loop but with closer inspection, however, the loop is still apparent. This looping effect for the compensated delay in comparison with the uncompensated is better explained using the envelope domain representation of dynamic power characteristics as shown in Figure 5.11. This triangular shape is due to the delay caused by the device itself when processing the signal. It is reported that a similar device can have delay of about 40ps and exhibits apparent triangular shape on its dynamic power characteristics [4]. As expected the dynamic power characteristics for compensated delay has the smallest size of the triangular artifact. Note that the dynamic characteristics shown in Figure 5.9 and 5.10 are performed with one power level.

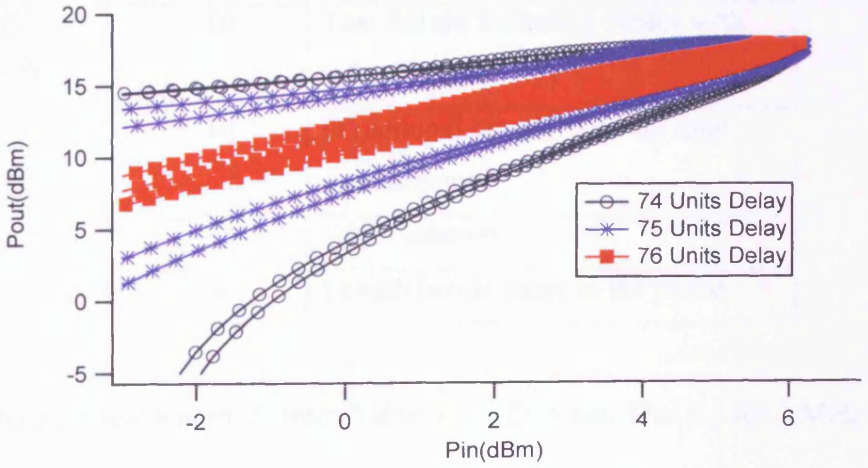


Figure 5.10: Envelope domain representation of the dynamic power characteristics for different delays

For passive load-pull system the main source of impedance variation or spread are the

frequency offset between the tones and the physical distance between the DUT and the tuning elements, probe and slug, of the tuner [5]. For slide screw mechanical tuners the phase delay variation or spread generated by the setup is as follows:

$$\Delta\theta = 0.024 \bullet L_T \bullet \Delta_F \qquad (5.1)$$

Where $\Delta\theta$ = phase variaton or spread (°)

L_T = electrical length between DUT and tuning element of tuner (cm)

Δ_F = frequency difference between the outermost tones (MHz)

The 0.024 coefficient value includes free space permittivity and permeability. It also includes the double electrical length to cater for transmission and reflection.

Table 5.1: Electrical length between DUT and the tuner element for on wafer measurement

Length/cm	Description
10	Test fixture including cables with teflon core (ε=1.9)
10	Directional coupler for real time measurement
2.5	GPC7 adapter
4	Length inside tuner to the probe

The total electrical length L_T from Table 5.1 is 26.5 cm. The Δ_F for 2 MHz modulation frequency, including IMD5 is 10 MHz. From Equation 5.1, the phase variation or spread:

$\Delta\theta = 0.024 \bullet 26.5 \bullet 10 = 6.36^{\circ}$

This effect of phase variation or spread is comparable with delay produce by the 10 ns

or one unit delay. Such a small electrical length can cause a dramatic effect in the envelope domain such as shown in Figure 5.9 and 5.10. If the modulation frequency is increased further similar to the frequency of the emerging fourth generation wireless standard, for example mobile WIMAX or LTE, including fifth inter-modulation distortions this can cause problematic error in load-pull measurement. In fact, if the modulation bandwidth goes up to 20MHz, the in-band bandwidth including IMD5 reaches to 100MHz span. Thus to achieve accurate characterisations, a constant impedance has to be maintained across the 100MHz bandwidth including IMD5.

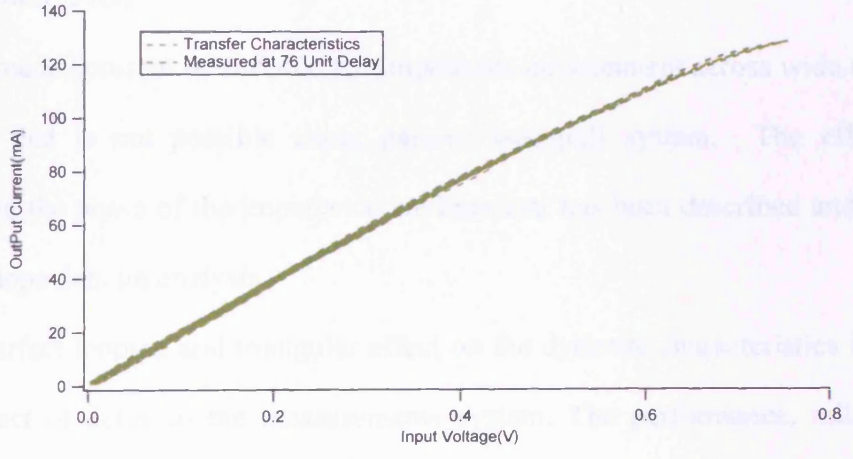


Figure 5.11: Envelope domain representation of dynamic transfer characteristics at different power levels

Figure 5.11 and 5.12 display compensated dynamic transfer characteristics and dynamic power characteristics for eight different power levels, respectively. These graphs show consistent results for different power levels. The results substantiate active envelope load-pull as a viable and robust tool for modern wideband power transistor characterization.

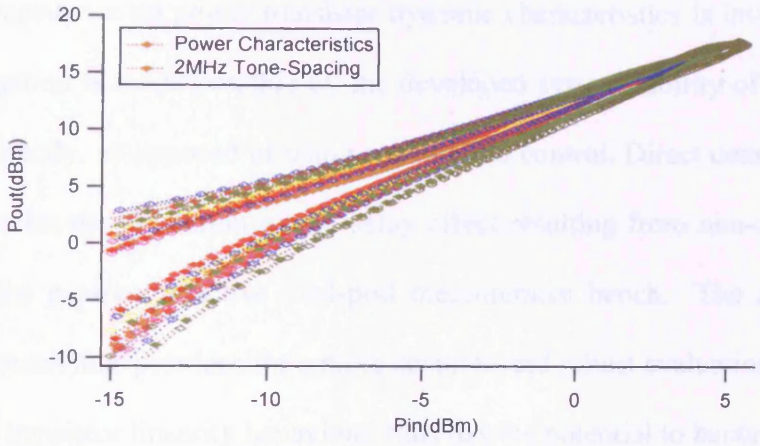


Figure 5.12: Envelope domain representation of dynamic power characteristics at different power levels

It can provide constant or variable RF impedance environment across wide modulation bandwidth that is not possible using passive load-pull system. The effect of the variations in the phase of the impedance environment has been described and illustrated using envelope domain analysis.

The imperfect looping and triangular effect on the dynamic characteristics is observed as an artifact of delay in the measurements system. The performance, reliability and robustness of the developed system will be useful for accurate modern power transistor characterization and hopefully will become one of the important tools in the advancement of power amplifier linearity investigations.

5.4 Chapter Summary

This chapter demonstrates the application of active envelope load-pull in characterising both power amplifier and transistor. Firstly, linearity contours of a packaged power amplifier are presented with minimum corruption due to the comprehensive wideband load impedance emulation including the inter-modulation distortions. The effect of the

RF in-band impedance on power transistor dynamic characteristics is investigated. This novel investigation is made possible by the developed systems ability of controlling the RF in-band directly, as opposed of using out-of-band control. Direct control of the load-emulation enables the emulation of the delay effect resulting from non-zero length that can exist in the passive or active load-pull measurement bench. The active envelope load-pull approach thus provides for a more accurate and robust evaluation of both power amplifier and transistor linearity behaviour, thus has the potential to become an important tool in the advancement of power amplifier linearity investigations and optimisation.

5.5 References

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CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

6.1 Conclusions

Load-pull provides a controlled and variable impedance environment for power amplifier or power transistor design and characterization. Utilising load-pull technique, by varying the emulated load impedance can help to determine device performance parameters including optimum output power, gain, efficiency or linearity. In this thesis, a load-pull capability is achieved that can provide constant impedance for modulated signals. Additionally, direct control of fundamental in-band impedances enables the effect of non-constant impedance to be investigated.

Load-pull system uses either passive or active approach. Each of the approaches has its own advantages and disadvantages. The emerging modern wireless communication standards, namely LTE and WIMAX, are increasing considerably the modulated bandwidth requirement of the load-pull measurement systems. To make matters worse, in order to characterise for linearity, including the significant fifth order inter-modulation distortions (IMD5s) requires five times the modulation bandwidth. The deficiency of both conventional passive and active load-pull becomes apparent as the modulation frequency increases to more than a few MHz, therefore, a new robust solution is necessary. Passive load-pull, for example, because of its physical realization, experiences loss from cable and

components. On the other hand, active load-pull suffers from limited bandwidth (closed-loop filter based architecture) and synchronization plus convergence issues (open-loop architecture). In addition, the load-pull systems, passive or active, suffer from delay problems due to the comparable signal wavelength with the measurement system component dimensions. From these perspectives, this thesis proposed, designed and developed a new digital controlled active envelope load-pull measurement system that is capable of properly handling wideband stimulus.

Unlike conventional load-pull architecture, the new envelope load-pull architecture can compensate for both amplitude loss and phase group delay. For fundamental frequency components, the compensation can be performed directly on in-band frequency components without resorting to conventional out-of-band control. Furthermore because it is baseband controlled close-loop architecture, as opposed to filter-based closed-loop, it is easier to control for delay compensation and can handle bigger bandwidth for wideband stimulus. Another important feature is that because it is a closed-loop system, it is also adaptive to the stimulus changes making it a very fast load-pull solution with excellent tracking capability accounting for the variable phase and magnitude usually employed in modern wireless communication standards. Furthermore, it should be able to support advance power amplifier architectures, for example envelope tracking with dynamic biasing. The closed-loop architecture also provides accurate real-time load emulation because no iteration is needed for load convergence. This real-time ability provides faster and safer load-pull with deterministic load emulation as opposed to iterative and fuzzy open-loop active load-pull load convergence.

In order to investigate the potential advantage of this new architecture verification measurements were performed. It was found that the feedback loop caused delay that induced the impedance variation. The delay was compensated successfully for presenting constant load impedance emulation across wide bandwidth. Experimental results show that the load-pull system can support up to 20 MHz overall bandwidth including the significant fifth order inter-modulation distortions (IMD5s) with at least 37 dB dynamic range.

The new load-pull system can provide not only constant impedance but also controlled impedance variation across the bandwidth. This new capability can provide better insight into factors modifying power amplifier and transistor performance, linear or non-linear, under wideband modulated stimulus. Typical AM-AM and AM-PM analysis including linearity contour plots were demonstrated. More advanced analysis is also performed in the envelope domain for the determining the effect of load impedance environment on the power transistor dynamic transfer characteristics. The envelope analysis works in the envelope domain i.e. by presenting the information in both time and frequency domain. As the modulated stimulus becomes more complicated, this approach enables more intuitive characteristics information to be extracted from the complicated output response, thus providing a better understanding of the non-linear behaviour. The envelope analysis is well suited for dissecting envelope load-pull measurement system results and it is reflected by the similarity in their names.

The developed digitally controlled active envelope load-pull has been experimentally shown to solve many problems associated with conventional load-pull systems, passive or active, and is capable of supporting wide bandwidth stimulus. It also improved on the

existing analogue controlled active envelope load-pull by providing more bandwidth and extra dynamic range necessary for capitalising on the real potential of the active envelope load-pull architecture to characterising modern wireless power transistors and amplifiers. Above all, it has opened up new research potentials of direct application of waveform engineering for multi-tone signal. This unprecedented capability can pave the way into systematic and robust investigation of power amplifier linearity and memory behaviour under realistic modulation conditions.

6.2 Future Works

Further possible improvements of the system are on the accuracy, load-pull capability and stimulus scaling (tone number and power). Furthermore, the digitisation of load-pull system provides a new avenue for cohesive integration of the discrete measurement system components being used in the measurement namely stimulus, the sampling scope and the load-pull. In addition to better synchronisation, the integration can lead to other advantages such as lower power requirement and lower system manufacturing cost.

6.2.1 Frequency Domain Control

Frequency domain control theoretically can improve system accuracy by compensating the phase and amplitude error of the presented load impedances. In addition, the accessibility of individual tone control opens up the possibility of purposely introducing impedance variation for emulating real world impedance matching networks. Replacing time domain complex multiplier unit, the frequency domain control consist of the Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) implementation. Since the signal is

known and repetitive, a window function for minimising spectral leakage is probably not necessary as long as the stimulus is synchronised properly with the FPGA board and the synchronisation is already existed in current implementation. The complex multiplier can be implemented inside the frequency domain or the existing time domain complex multiplier can be utilised. If the latter is the case, frequency domain control will only be used to fine tune the impedances in frequency domain. In a nutshell, frequency domain control can be used to either eliminate the variation on the impedance tones for better accuracy or improving the load-pull capability by emulating real world impedance matching network by controlling the tones individually.

6.2.2 Multi-sine Stimulus Characterisations

The existing system has low bandwidth limitation due to the baluns at the ADC/DAC. The multi-tone stimulus can only get through if there is sufficient bandwidth gap in the middle of the spectrum. Realistic power amplifier and transistor measurement may require multi-tone stimulus very similar to the modern wireless modulation technique, for example fifty one tones multi-sine emulating CDMA signal. Given 2 MHz modulation bandwidth, the separation between tones is 40 kHz which is smaller than the minimum bandwidth limitation. Since the load-pull digital control is using homodyne direct conversion architecture it is necessary to offset the LO frequency in order to allow multi-tone stimulus with small bandwidth spacing to get through albeit the supported measurement system bandwidth will be reduced.

Another option is to adopt heterodyne architecture that produce IF that can pass through the baluns. This heterodyne architecture is more complicated and the I/Q demodulation

and modulation must be performed inside the digital domain (FPGA). The advantage of this approach is that there will be no impairment due to the absence of analogue based I/Q modulation and demodulation process.

6.2.3 Digital Based Multi-Harmonics Active Envelope Load-Pull

Analogue based multi-harmonics active envelope load-pull is already in place for measuring narrowband signals. Currently the digital based implementation can only cater for in-band frequency investigation. The same technique can also be extended for out-of-band control, baseband and the other harmonics, for fully characterising non-linear systems. Similar to in-band control, the out-of-band controller should be able to handle multi-tone signals directly and comprehensively. Coupled with the feasibility of individual tone control in frequency domain described in previous section, the multi-harmonic active envelope load-pull can potentially become the ultimate waveform engineering tool enabling first-pass power amplifier design.

6.2.4 Time Domain Pre-distortion

Pre-distortion in time domain can effectively neutralised non-linear power amplifier (AM-AM and AM-PM distortions) being used to pre-amplify the reflected waves especially in high power application. The implementation technique will be similar to the power amplifier baseband digital pre-distortion technique. The feedback loop amplifier is normally placed after the modulator producing RF signal that contains the up-converted modified I and Q channels. Thus a mechanism to tap the output of the loop amplifier back to the FPGA in order to compare the delayed version of the input and the output of the loop

amplifier. A Look-up table (LUT) is then used to compensate for any non-linear deviation produced by the loop amplifier using the same complex multiplication technique on both of I and Q channels that already being used by the digital control module of the active envelope load-pull.

6.2.5 Hybrid Load-Pull and Measurement System

The other potential further work in the long term is to unify the main measurement system components being used in the large signal measurement and load-pull system. Ultimately the stimulus, the sampling scope and the load-pull hardware functionality can be combined into one cohesive and integrated hybrid load-pull and measurement system or *waveform engineering system.* This integration can simplify synchronisation due to all the main equipments being based on the same mother board (FPGA).

Furthermore, most of the recommended further works can potentially be realised and implemented on the same FPGA board because the FPGA resource utilisation for this work is small (less than 10%) as shown in Chapter 3. If a single FPGA board is not enough it is a simple matter to use multiple FPGA boards and synchronised them together for seamless digital control capability. This potentially can provide lower power usage requirement for more environmentally friendly measurement system. Last but not least, integration can provide lower cost availability of waveform engineering system hence probably increases its adoption as a potent power amplifier and other non-linear microwave devices characterisation and measurement tool around the world.

APPENDIX A

VERILOG CODES FOR POLARITY INVERSION

```
module posnegclk(in,sign,out,clk);
input clk;
input [11:0]in;
input [0:0]sign;
output reg [11:0]out;

reg [11:0]buff1;

always@(posedge clk)
begin

if (sign[0]==0)
begin
out=in;
end


else
begin
buff1[11:0]=~in+1;
out=buff1;
end

end
endmodule
```

APPENDIX B

VERILOG CODES FOR TRUNCATION AND SIGNED TO UNSIGNED CONVERSION

```
module Conv32to14(in,out);
input [31:0]in;
output reg [13:0]out;
reg [13:0]buff1;
reg [31:0]buff2;

always @(1)

begin

if(in[31:31]==0)
begin
buff2=in;
buff1[13:0]=buff2[16:3];
out=buff1+4096;
end

else

begin
buff2=~in+1;
buff1[13:0]=buff2[16:3];
out=4096-buff1;
end
end
endmodule
```

APPENDIX C

ADC STRATIX II PIN-OUTS

ADC A	
Signal Name	Stratix II Pin
adcA_D0 (LSB)	D1
adcA_D1	D2
adcA_D2	E3
adcA_D3	E4
adcA_D4	E1
adcA_D5	E2
adcA_D6	F3
adcA_D7	F4
adcA_D8	F1
adcA_D9	F2
adcA_D10	G3
adcA_D11 (MSB)	G4

ADC B	
Signal Name	Stratix II Pin
adcB_D0 (LSB)	G1
adcB_D1	G2
adcB_D2	J3
adcB_D3	J4
adcB_D4	H1
adcB_D5	H2
adcB_D6	J1
adcB_D7	J2
adcB_D8	K3
adcB_D9	K4
adcB_D10	K1
adcB_D11 (MSB)	K2

APPENDIX D

DAC STRATIX II PIN-OUTS

DAC A	
Signal Name	Stratix II Pin
dacA_D1 (MSB)	W4
dacA_D2	W5
dacA_D3	Y6
dacA_D4	Y7
dacA_D5	Y8
dacA_D6	Y9
dacA_D7	Y10
dacA_D8	Y11
dacA_D9	AB5
dacA_D10	AB6
dacA_D11	AA10
dacA_D12	AA11
dacA_D13	AA6
dacA_D14 (LSB)	AA7

DAC B	
Signal Name	Stratix II Pin
dacA_D1 (MSB)	U5
dacA_D2	U6
dacA_D3	U10
dacA_D4	U11
dacA_D5	V9
dacA_D6	V10
dacA_D7	V6
dacA_D8	V7
dacA_D9	V4
dacA_D10	V5
dacA_D11	W8
dacA_D12	W9
dacA_D13	W6
dacA_D14(LSB)	W7

APPENDIX E

A SINGLE POINT LOAD-PULL ACROSS MODULATION BANDWIDTH

Modulation	In-band	Freq (MHz)	Magnitude	Phase (°)	Real	Imaginary
1.6 MHz modulation bandwidth (8 MHz)						
	IMD5U	4	0.121	50.12	-0.09	-0.08
	IMD3U	2.4	0.110	63.64	-0.10	-0.05
	F2	0.8	0.108	78.33	-0.11	-0.02
	F1	-0.8	0.118	65.45	-0.11	-0.05
	IMD3L	-2.4	0.106	77.19	-0.10	-0.02
	IMD5L	-4	0.101	79.69	-0.10	-0.02
2 MHz modulation bandwidth (10 MHz)						
	IMD5U	5	0.115	78.06	-0.11	-0.02
	IMD3U	3	0.111	80.62	-0.11	-0.02
	F2	1	0.113	85.49	-0.11	-0.01
	F1	-1	0.125	67.64	-0.12	-0.05
	IMD3L	-3	0.127	70.57	-0.12	-0.04
	IMD5L	-5	0.131	73.46	-0.13	-0.04
2.5 MHz modulation bandwidth (12.5 MHz)						
	IMD5U	6.25	0.107	83.39	-0.11	-0.01
	IMD3U	3.75	0.109	76.66	-0.11	-0.03
	F2	1.25	0.110	78.92	-0.11	-0.02
	F1	-1.25	0.122	64.76	-0.11	-0.05
	IMD3L	-3.75	0.126	69.12	-0.12	-0.04
	IMD5L	-6.25	0.139	63.15	-0.12	-0.06
4 MHz modulation bandwidth (20 MHz)						
	IMD5U	10	0.086	79.44	-0.08	-0.02
	IMD3U	6	0.109	74.73	-0.11	-0.03
	F2	2	0.112	78.36	-0.11	-0.02
	F1	-2	0.121	69.14	-0.11	-0.04
	IMD3L	-6	0.135	70.50	-0.13	-0.04
	IMD5L	-10	0.125	64.99	-0.11	-0.05
Average			0.116	72.64		
Load-pull Reference Point	B2 POINT		0.119	71.36	-0.11	-0.04